

# A Low-Power Cochlear Implant System

by

Michael W. Baker

Submitted to the Department of Electrical Engineering and Computer  
Science

in partial fulfillment of the requirements for the degree of

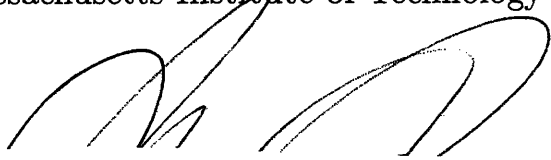
Doctor of Philosophy in Computer Science and Electrical Engineering

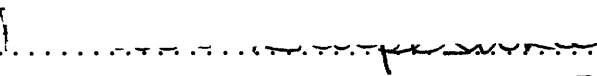
at the

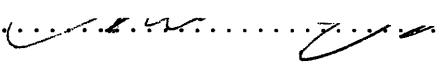
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2007

© Massachusetts Institute of Technology 2007. All rights reserved.

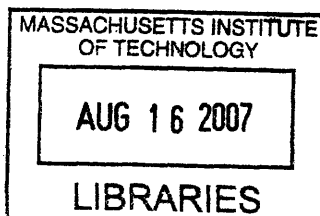
Author   
.....  
Department of Electrical Engineering and Computer Science  
May 25, 2007

Certified by   
.....  
Rahul Sarpeshkar  
Associate Professor, Department of Electrical Engineering and  
Computer Science  
Thesis Supervisor

Accepted by   
.....  
Arthur C. Smith

**ARCHIVES**

Chairman, Department Committee on Graduate Students





# A Low-Power Cochlear Implant System

by

Michael W. Baker

Submitted to the Department of Electrical Engineering and Computer Science  
on May 25, 2007, in partial fulfillment of the  
requirements for the degree of  
Doctor of Philosophy in Computer Science and Electrical Engineering

## Abstract

Cochlear implants, or bionic ears, restore hearing to the profoundly deaf by bypassing missing inner-ear hair cells in the cochlea and electrically stimulating the auditory nerve. For miniaturized cochlear implants, including behind-the-ear (BTE) models, power consumption is the chief factor in determining cost and patient convenience.

This thesis reports on the design of a low-power bionic ear system by addressing three critical signal and power processing subsystems in low-cost CMOS ICs. First, the design of a low-power current-mode front-end for subminiature microphones demonstrates 78dB dynamic range performance with attention to RF noise and supply immunity. Second, hearing-impaired patients need strategies that decide intelligently between listening conditions in speech or noise. This work describes an automatic gain control (AGC) design which uses programmable hybrid analog-digital current-mode feedback to implement a dual-loop strategy, a well-known algorithm for speech in noisy environments. The AGC exhibits level-invariant stability, programmable time constants and consumes less than  $36\mu W$ . Third, a feedback-loop technique is explored for analyzing and designing RF power links for transcutaneous bionic ear systems. Using feedback tools to minimize algebraic manipulations, this work demonstrates conditions for optimal voltage and power transfer functions. This theory is applied to a bionic implant system designed for load power consumptions in the 1mW — 10mW range, a low-power regime not significantly explored in prior designs. Link efficiencies of 74% and 54% at 1-mm and 10-mm coil separations, respectively, are measured, in good agreement with theoretical predictions.

A full cochlear implant system with signal and power processing is explored incorporating the front-end, AGC, and RF power link, as well as analog signal processing channels. This design uses channel data to feedforward program the just-needed electrode power level. My implant system consumes 3mW of power for all audio processing and a stimulation power of 1mW. A fixed-power version of this system dissipates 2.2mW for 1mW of internal stimulation power. As many commercial systems with similar specifications consume 40mW – 80mW, this effort promises a significant reduction in cochlear implant power consumption and cost.

Thesis Supervisor: Rahul Sarpeshkar

Title: Associate Professor, Department of Electrical Engineering and Computer Science



## Acknowledgments

*...une oeuvre d'homme n'est rien d'autre que ce long cheminement pour retrouver par les détours de l'art les deux ou trois images simples et grandes sur lesquelles le coeur, une première fois, s'est ouvert.*

Albert Camus – *L'envers et l'endroit*

I have found help and support for my work in many forms during my graduate career. I'd like to thank my thesis committee: First, Professor Rahul Sarpeshkar, whom I have worked with in one way or another since 1999, has inspired me with his persistent need for insight and clarity. Second, Professor Joel Dawson and Professor David Perreault, have been very helpful throughout the process with technical and writing advice.

I would like to thank all the members of the Analog VLSI and Biological Systems Group, past and present, for their excellent technical work and encouragement. Also, the staff of the Research Laboratory for Electronics and the Electrical Engineering and Computer Science Department have provided a superb environment for exciting research.

I would like to thank the Advanced Bionics Corporation and the Boston Scientific Corporation for their support of our research into future cochlear implant technologies.

Finally, I would like to thank my family: without their love, support, curiosity, and great personal sacrifice, I would not have had the opportunity to succeed at MIT over the past 10 years. Also, to my friends, much thanks for their support and almost infinite patience with me over the years.



# Contents

<b>1</b>	<b>Introduction</b>	<b>23</b>
1.1	Hearing Loss and Hearing Instruments . . . . .	23
1.2	Cochlear Implant Systems . . . . .	24
1.2.1	Front-End Circuits . . . . .	27
1.2.2	Power Transfer to the Implanted Stimulator . . . . .	29
1.3	Thesis Outline . . . . .	31
<b>2</b>	<b>Low-Power Current-mode Microphone Preamplifiers for Mixed-Signal Systems</b>	<b>33</b>
2.1	Microphones for Bionic Implants and Hearing Aids . . . . .	34
2.2	Sense-Amplifier Topology . . . . .	37
2.2.1	Frequency-Dependent Feedback . . . . .	38
2.2.2	Split-Frequency Feedback . . . . .	40
2.3	Power-Supply Rejection . . . . .	42
2.4	Experimental Results . . . . .	46
2.4.1	Gain . . . . .	47
2.4.2	Power Supply Rejection . . . . .	51
2.4.3	Noise Performance . . . . .	51
2.4.4	Linear Range . . . . .	55
2.5	Summary . . . . .	58
<b>3</b>	<b>Low-Power Single-Loop and Dual-Loop AGCs for Bionic Ears</b>	<b>61</b>
3.1	Some Properties of AGCs . . . . .	62

3.1.1	Feedforward vs. Feedback Gain Control . . . . .	63
3.2	Single-Loop AGCs . . . . .	65
3.2.1	Variable Gain Amplifier . . . . .	66
3.2.2	Translinear Circuit Design . . . . .	72
3.2.3	Translinear Circuit Offsets . . . . .	74
3.2.4	Log-Linear Controller Properties . . . . .	74
3.3	Dual-Loop AGC . . . . .	77
3.3.1	The Dual-loop algorithm . . . . .	78
3.3.2	Circuit Implementation of the Dual-loop Algorithm . . . . .	80
3.4	Experimental Results . . . . .	83
3.4.1	Variable Gain Amplifier . . . . .	87
3.4.2	Single-Loop AGC . . . . .	90
3.4.3	Dual-Loop AGC . . . . .	92
3.5	Summary . . . . .	96
<b>4</b>	<b>Feedback Analysis and Design of RF Power Links for Low-Power Bionic Systems</b>	<b>99</b>
4.1	Basic Model of Coupled Resonators in an RF Link . . . . .	102
4.1.1	Feedback Analysis . . . . .	104
4.1.2	Root Locus Analysis . . . . .	105
4.1.3	Coupled Resonator Voltage Transfer Function . . . . .	108
4.1.4	Limits to Energy Efficiency . . . . .	109
4.2	System Design . . . . .	112
4.2.1	Resonator Design – Load Design . . . . .	117
4.2.2	Driver Design . . . . .	118
4.3	Measured Performance . . . . .	121
4.3.1	Efficiency . . . . .	126
4.4	Summary . . . . .	127
<b>5</b>	<b>A Low-Power Transcutaneous Cochlear Implant System With Feed-forward Power Control</b>	<b>131</b>

5.1	Analog Bionic Ear Processing (ABEP) System . . . . .	132
5.1.1	Front-end Signal Processing . . . . .	132
5.1.2	Programmable Processing Channel . . . . .	134
5.2	A Transcutaneous Bionic Ear Implant . . . . .	136
5.2.1	Feedforward Power Control . . . . .	137
5.2.2	Feedforward Controller Circuits . . . . .	141
5.3	Results . . . . .	143
5.3.1	Feedforward Control Performance . . . . .	145
5.3.2	Fixed Power Performance . . . . .	147
5.4	Summary . . . . .	149
5.5	Lessons of this Thesis . . . . .	149
5.5.1	Low-Power Analog Front End . . . . .	150
5.5.2	Dual-loop AGC . . . . .	150
5.5.3	Transcutaneous Inductive Power Links . . . . .	151
5.5.4	Transcutaneous Bionic Ear System . . . . .	152
<b>A</b>	<b>Comparison of Passive and Active Supply Filters</b>	<b>153</b>
<b>B</b>	<b>Optimal Sizing of the Power Switch in the Class-E Power Amplifier</b>	<b>155</b>
B.1	nMOS Switching Device . . . . .	155
B.2	Losses in Primary Circuit . . . . .	156
B.2.1	Switching Considerations . . . . .	156
B.3	Design Performance . . . . .	159
B.4	Sizing the Device for Optimal Performance . . . . .	159
B.5	Efficiency Comparison . . . . .	163
<b>C</b>	<b>Class-D Amplifier Design for Transcutaneous Power Links</b>	<b>165</b>
C.1	Class-D Power Amplifier . . . . .	165
C.1.1	Class-D Design and Optimization . . . . .	166
C.2	Simulation Results . . . . .	169
C.2.1	Efficiency . . . . .	169



# List of Figures

1-1	A behind-the-ear (BTE) cochlear implant is shown. An external microphone and speech processor process sound signals. A transmitter coil sends power and data into the implanted unit which stimulates the electrode array. Figure used with permission from the National Institute on Deafness and Other Communication Disorders ( <a href="http://www.nicdc.nih.gov">www.nicdc.nih.gov</a> ).	25
1-2	The signal processing and power transfer stages in a typical cochlear implant system. . . . .	25
1-3	Audio front-end architectures with automatic gain control for reducing dynamic range. . . . .	28
1-4	The coupling between inductors $L_1$ and $L_2$ is modeled as two current dependent voltage sources. . . . .	30
2-1	Subminiature electret circuit. (a) Low-noise depletion-mode FET device shown with source resistance, $R_S$ . A large gate resistance is also shown to indicate that the gate is incrementally grounded at low frequency. (b) Small-signal model of the internal structure of the microphone, including the active device and parasitic gate and source resistances. . . . .	35
2-2	Conceptual block diagram of the power-supply noise feedthrough. The summer indicates the summing of currents contributing to the source node of the FET buffer. . . . .	35
2-3	A sense amplifier can be used to bias the drain of the buffer JFET as well as provide pre-amplification. . . . .	37

2-4	Frequency dependent feedback networks are shown which can mitigate the effects of DC current in the feedback path. . . . .	38
2-5	Sense amplifier topology employing split-frequency feedback. The DC voltage drop in the feedback load is proportional to the DC output current of the amplifier and is regulated to zero by cancelling the microphone buffer's DC current with feedback DC current from $M_1$ . . .	41
2-6	Small-signal block diagram for the design presented in Fig. 2-5. . . .	42
2-7	Power-supply decoupling mechanism. (a) Explicit gate-source capacitors, $C_{GS,1}$ and $C_{GS,2}$ , and biasing of p-gates through high-impedance elements, $z_A$ , make $M_1$ and $M_2$ behave as small-signal large resistances. (b) A bypass capacitor $C_{bypass}$ filters the supply voltage before it can affect the bias at $i_{D,2}$ . . . . .	44
2-8	Small-signal model of $M_1$ in Figure 2-7. . . . .	44
2-9	Complete circuit topology including the supply decoupling networks. The microphone structure is shown at the bottom left in the dashed box.	48
2-10	Die photo of the current-mode pre-amplifier. The chip is a $2.2mm \times 2.2mm$ chip built in a $1.5\text{-}\mu m$ process. . . . .	49
2-11	Frequency response to acoustic excitation with the output supply coupling response normalized to 1-Vpp variation of the supply. The supply rejection performance for various bypassing capacitances is shown. . .	50
2-12	Supply coupling for frequencies up to 26MHz. . . . .	52
2-13	High-frequency signals are filtered most effectively from the output in the presence of a large bypass capacitor. A static protection resistor in the chip's pads limited the attenuation of the decoupling path to -64dB.	53
2-14	Without microphone noise, feedback and operational amplifier contribute $80\text{-}90\text{ nVrms}/\sqrt{Hz}$ . The microphone buffer noise dominates when audio input is on. The $1/f$ nature of the microphone-on characteristic is due in part to the $1/f$ noise of the DC biasing structure. (Note this figure had a scale error in the published version [30]). . .	54
2-15	Distortion products for 1kHz peak output with 1% distortion. . . . .	55



2-16	Distortion products for 3kHz peak output with 1% distortion. . . . .	56
2-17	Dynamic range versus frequency for acoustic inputs. . . . .	57
3-1	Single-loop controller. The envelope signal from the rectifier and peak detector, $i_{ED}$ and the translinear controller signal, $i_{GAIN}$ , are shown. A minimum-current circuit enforces a maximum gain by comparing the gain current $i_{GAIN}$ with $I_{KNEE}$ and switching the smaller of the two to the VGA. . . . .	64
3-2	VGA block diagram. The ratio of currents $i_{GAIN}$ and $I_{REF}$ in the input and output amplifiers, respectively, determine the gain of the circuit. The reference current level $I_{REF}$ is usually about 100nA, and the gain current $i_{GAIN}$ is usually from 100nA – 1.2μA. . . . .	67
3-3	One of the transconductors from the VGA circuit. The transconductor uses wide-linear-range circuit techniques – bulk inputs, gate-degeneration, and bump linearization described in the text [38]. . . .	68
3-4	A translinear circuit implementing an inverse exponential is computed using a pseudo-linear voltage divider. The voltage divider sums the influence of the logarithm of the envelope current, $i_{ED}$ , with the reference current, $I_{REF}$ . Bipolar transistors are used to avoid above-threshold effects in MOS devices. A filter comprising a capacitor $C_T$ and an nMOS cascode transistor $M_1$ is included at the output node. . . . .	73
3-5	Diagram of linearized loop. The loop variables correspond to small-signal envelopes, $e_{in}$ and $e_{out}$ , or rectifier or control currents, $i_{ed}$ and $i_{gain}$ . . . . .	76
3-6	An outline of the dual-loop operation on a hypothetical input envelope. Note that the hold-timer condition informs the release of the slow envelope filter. . . . .	79
3-7	Circuit blocks for the dual-loop controller, including the charge-pump structure of the hold-timer. . . . .	82

3-8	Dual-loop controller circuits including the current comparator (A) employing a high impedance current subtractor and a voltage amplifier. The current switching circuit (B) uses two pMOS triode switches to choose between input currents $I_1$ and $I_2$ . A charge-pump implements the hold-timer (C). To determine the state of the charge-pump voltage, $V_{HoldTimer}$ , two open-loop voltage amplifiers are included. The selectable attenuator for the fast filter current is shown in (D). State-logic shown in (E) is included to prevent over-charging or under-charging conditions for the hold-timer. The W/L's of all transistors are $8\mu m/3.2\mu m$ . The current bias for the inverters, $I_{BIAS}$ , was chosen to be approximately 30nA. . . . .	84
3-9	Single-loop controller AGC chip. . . . .	85
3-10	Dual-loop controller AGC chip. This die includes a parallel digital programming channel for six separate parameters in the dual-loop design.	86
3-11	Maximum output signal of the variable gain amplifier for 1% THD at varying gain levels. The test frequency was 1-kHz. . . . .	88
3-12	Total output noise at the $v_{OUT}$ node is integrated from 30-Hz to 100-kHz. The solid line represents white noise modeled from Eq. 3.6. Theory and data curves diverge at high gains owing to the relatively larger presence of $1/f$ noise at these bias currents, which is not modeled in Eq. 3.6. . . . .	89
3-13	Maximum instantaneous output SNR versus gain for a 1 % distortion limit. Note that this is a decreasing function of the gain as more gain increases the output noise. Theory from Eq. 3.8 is shown in the solid line with a constant linear range, $V_L$ . . . . .	90
3-14	Compression curves for varying $\alpha = \{1.07, 1.16, 1.33, 1.43, 1.67\}$ . A knee was imposed using the max circuit to enforce maximum gain current, $A_V = 600nA$ . These data were taken from the single-loop AGC.	91
3-15	Closed-loop time constants for the single-loop controller. . . . .	93

3-16	Closed-loop time constants for the single-loop controller versus input level. The open-loop attack time constant $\tau_a$ was set to 80ms. . . . .	94
3-17	A transient response of the dual-loop controller. The input waveform $v_{IN}$ is designed to excite several of the relevant conditions for the hybrid controller. The background sound is a 1- $kHz$ sinusoid with tone-bursts presented at 0.5s and 2.5s. At 2.75s, a larger tone is presented with 100ms duration, intended to represent a loud transient and trigger the fast response loop. The output voltage $v_{OUT}$ is shown below the input voltage trace and indicates slow-loop adaptation in gain for each tone-burst. The gain release does not begin until the hold-timer has discharged to its resting level. This can be seen in the gain current shown at the bottom. When the loud transient occurs, at 2.75s, the gain is reduced rapidly, corresponding to the fast-loop attack time constant. . . . .	95
4-1	An example of a low-power bionic implant system is shown. . . . .	102
4-2	Inductively coupled series-parallel resonators. Coupling between the inductors is modelled with dependent voltage sources $sMi_1$ and $sMi_2$ . . . . .	103
4-3	Feedback diagrams for coupled resonators in Figure 4-2. The top diagram (a) shows the loop diagram under all frequencies. The bottom diagram (b) shows an approximate loop diagram under resonant conditions $\omega = \frac{1}{\sqrt{L_1C_1}} = \frac{1}{\sqrt{L_2C_2}}$ . . . . .	104
4-4	Root locus diagrams are shown for two resonator cases. In (a), the resonators are identical. A loaded resonator case (b) will have a higher damping factor due to energy lost to the rectifier. In this case the poles move together before splitting from the constant- $\omega_n$ circle. . . . .	107
4-5	An overall Nyquist diagram of $L(s)/k^2$ is shown in (a) and detail near the origin is shown in (b). As the frequency approaches $\omega_n$ the Nyquist plot approaches the $180^\circ$ point with magnitude $Q_1Q'_2$ . For $L(s) = -1$ , and this phase condition we must have $k = k_c$ . . . . .	107

4-6	The test setup used for inductive power transfer system tests is shown. The coil separation can be adjusted and measured with millimeter accuracy. Coil rotation can also be explored for both the primary and secondary coils. The electronic boards are glued to Delrin scaffolding with Teflon screws used to bind the various portions of the scaffold. .	113
4-7	The left plot (a) shows how the closed-loop poles move as the coil distance is changed. At some coil separation, the poles begin to move apart and a low-frequency high-Q and high-frequency low-Q peak are observed. The right (b) plot shows the voltage peak at resonance as I change the coil coupling factor. The peak occurs at roughly $k_c \sim 0.1$ .	114
4-8	Efficiency of power transfer between coupled resonators for varying loading. The data I show were produced by ignoring switching losses in a discrete Class-E amplifier implementation. . . . .	115
4-9	The coupling factor $k$ for coils of radius 14mm are shown. These measurements were taken using the test setup shown in Figure 4-6. . . . .	116
4-10	A switching power driver (Class-E) is shown with the primary circuit and a one-shot control loop. The Class-E supply voltage, $V_{DD,CE}$ , controls the power level, while the clock, comparator, NOR gate, one-shot circuit and latch control the gate drive timing. . . . .	119
4-11	A simple comparator for the Class-E controller. The comparator triggers the NOR gate when $v_d$ approaches zero volts. The device sizes were ratioed to obtain a low voltage threshold. The threshold is intentionally not exactly at ground to allow for some error compensation due to delays in my control scheme. . . . .	120
4-12	Die photograph of the $0.5\mu\text{m}$ power systems chip. This chip includes two power switches and two independent controllers. A clock generator, for off-chip crystals, as well as a feed-forward data system (not discussed in this chapter) are also included on the chip. . . . .	122

4-13	System waveforms, including the clock, gate-driver signal, Class-E drain voltage $v_d$ , secondary voltage $v_2$ , and rectified voltage $V_{RECT}$ are shown for a 4mm coil separation condition. . . . .	123
4-14	Three cases are shown for the Class-E drain voltage $v_d$ . Note that the switch timing has adapted slightly to reduce the amount of $fC_s v_d^2$ wasted power under the 1mm and 10mm conditions. Furthermore, the action of the protection diode can be seen in the $d = 10mm$ case where the drain voltage has dropped below ground. . . . .	124
4-15	Variation in the rectified output voltage is shown for two power driver voltage levels. The rectified voltage variation is less than 16% for all cases. . . . .	125
4-16	A comparison between the asymptotically efficient coupled resonator power transfer system ( $Q_1 = 35, Q_2 = 90$ ) is shown with my system. The top curve indicates the maximum possible efficiency for an adapting load condition (Equation 4.15). The dashed theory curve indicates efficiency for the fixed loading condition, $Q_{L,opt}$ , (Equation 4.13). My system performance is shown for 10mW and 1mW operation. . . . .	128
4-17	A plot of the efficiency is shown for a sweep in the power level by changing the class-E supply voltage. The efficiency of each mechanism is shown for comparison. At low power levels, controller power and losses in the rectifier contribute most to inefficiency of the system. . .	129
5-1	An analog bionic ear processor chip architecture is diagrammed. The signal path consists of a programmable front-end and 16 programmable channels. The bias generator connections to each of the analog blocks are not shown to avoid clutter on the figure. . . . .	133

5-2	The analog bionic ear processing chip die photo shows each of the signal processing and biasing stages. This die is $10mm \times 10mm$ and requires only four off-chip components to operate – an off-chip microphone and two gain-setting resistors are needed as well as a clock source. This chip operates from a 2.8V supply with only $90\mu A$ of current. . . . .	135
5-3	An outline of the transcutaneous implant architecture using the ABEP processor and power system chip. Clock generation for the power amplifier and the ABEP is done by the power system chip. The ABEP chip accepts audio input from microphones and auxiliary sources, programming bits from an external memory, and sends CIS output bits to the power system chip for feedforward programming of the just-needed power for the implanted unit. . . . .	136
5-4	A simplified model of the internal electrical load is shown for a simple CIS stimulation strategy. An array of $N$ electrodes is stimulated with a biphasic current pulses of length $T_{Pulse} \times 2$ . Each electrode is stimulated with a repetition frequency of $f_{CIS}$ and each pulse can have a range of current intensities at each electrode from $100\mu A$ to $1mA$ . . . . .	138
5-5	Block diagram of feedforward control for just-needed power. . . . .	140
5-6	Feedforward circuits control the power level dynamically. Circuits are described in the text. . . . .	142
5-7	A photo of my implant system test board shows the analog bionic ear processor (ABEP) and the power system chip. A programming interface allows configuration of 86 patient parameters. The secondary board with the rectifier and resistive load model are not shown. . . .	144
5-8	The off-the-shelf switching regulator configuration is shown with the output network and feedback control from the power chip. The battery and output supply voltages were bypassed with ceramic and electrolytic capacitors to improve ripple rejection and stability. . . . .	145

5-9	A sweep of the power level is shown for the 16 possible input codes. The top trace shows the regulator voltage, $V_{REG}$ . The bottom trace shows the power dissipated in the internal stimulator for all code settings.	146
5-10	A breakdown of the power consumption in the implant board is shown for a feedforward power control case at 1mm coil separation. Constant power dissipations; ABEP, clock generator, and control circuits, were measured and assumed to be constant for all operating power levels. The <b>Useful Power</b> represents the total power delivered to the load, $R_L$ , plus the constant power dissipation terms. . . . .	147
5-11	A breakdown of the power consumption in the implant board is shown for a fixed power level case at 1mm coil separation. Constant power dissipations; ABEP, clock generator, and control circuits, were measured and assumed to be constant for all operating power levels. The <b>Useful Power</b> represents the total power delivered to the load, $R_L$ , plus the constant power dissipation terms. . . . .	148
B-1	The conditional linear circuits for a class-E amplifier are shown. On the left, the FET-off condition is shown with current from the radio frequency choke (RFC) charges the output network. On the right, the FET-on condition is shown. In this condition the output capacitance $C_S$ is shorted to ground, the tank self-resonates and the RFC is fluxed by connecting it to ground. . . . .	157
B-2	The top set of traces show a breakdown of conduction and switching losses in the Class-E amplifier for a useful power of 1mW. The conduction loss in the switch dominates the losses in the system for the $M = 100$ device. The bottom graph shows the efficiency from Eq. B.4 for a 1mW load power. . . . .	160
B-3	A set of efficiency traces are shown for various coupling conditions. The optimal device sizing is different depending on coil separation due to changing current levels in the primary circuit. . . . .	161

B-4	A breakdown of conduction and switching losses in the Class-E amplifier for a useful power of 1mW. The conduction loss in the switch dominates the losses in the system for the $M = 200$ device. The bottom graph shows the efficiency from Eq. B.4 for a 1mW load power. .	162
B-5	The traces from Figure 4-16 are shown with an additional curve for the maximum possible efficiency given an improved primary quality factor, $Q_1$ , from 35 to 51. The improvement in efficiency is anywhere from 4% to 7% over the range of couplings. . . . .	163
C-1	A bridged Class-D topology is shown. Active devices hard-switch the drain nodes, $v_{d1}$ and $v_{d2}$ . Power level can be controlled by delaying the switching waveform by a phase angle, $\delta$ . . . . .	166
C-2	The efficiency, computed from Equation C.1, is plotted for various device sizings. Losses in the rectifier were not included in this calculation.	167
C-3	A breakdown of the loss mechanisms is shown as the coil coupling is changed for 10mW of power delivered to the load. This calculation assumed that maximum power was being delivered, i.e. $\delta = 0^\circ$ . . . .	168
C-4	Power level and efficiency are shown for various phase angles, $\delta$ . . . .	170



# List of Tables

2.1	Noise and Distortion Performance of Low-Power Microphone Frontend.	56
2.2	Overall Specifications for Low-Power Microphone Frontend. . . . .	56
3.1	Dual-Loop System Programming Properties . . . . .	87
3.2	Single-Loop Controller Power Consumption . . . . .	87
3.3	Dual-Loop Controller Power Consumption . . . . .	88
4.1	Efficiency Test Setup Parameters . . . . .	112
4.2	Secondary Resonator Design . . . . .	117
4.3	Final System Specifications . . . . .	127
4.4	Final System Performance . . . . .	128
5.1	Programming variables in ABEP front-end and Single-loop AGC . . .	133
5.2	Programming variables in each ABEP channel . . . . .	135
5.3	Approximate CIS/Electrode Parameters . . . . .	138
5.4	Total Power Consumption for 1mW Load Power of Feedforward Con- trol Bionic Ear System . . . . .	147
5.5	Total Power Consumption for 1mW Load Power of Fixed Power Bionic Ear System . . . . .	149
A.1	Some Figures of Merit for Active and Passive R-C Supply Filters . . .	154
C.1	Class-D Power Driver Simulation Parameters . . . . .	169



# Chapter 1

## Introduction

This thesis reports on progress on ongoing problems in implanted electronics for bionic hearing prostheses. Among the myriad challenges that face implanted electronics designers, I have chosen to focus on areas that will improve bionic implants for the deaf. As I will describe in greater detail below, the power consumption of these devices is the chief determining factor in unit cost. By focusing on the power consumption of the entire system, I am making an effort to reduce the cost of cochlear implant technology making it an accessible and economically feasible choice for more people all over the world.

Hearing impairment affects almost 10% of individuals in the industrialized world [1]. The design of hearing instruments is, therefore, of great importance to society. Deaf patients with more than 70 – 80dB of hearing loss require a cochlear implant, or bionic ear, to hear and cannot use hearing aids [2]. Cochlear implants directly stimulate the auditory nerve with electrical current using 8 – 20 electrodes surgically implanted as a spiralling array in the patient’s cochlea.

### 1.1 Hearing Loss and Hearing Instruments

Various human hearing impairments require different strategies for treatment. While a healthy listener can comfortably detect sounds over a wide dynamic range (90 to 100 dB) of sound pressure levels, damage, aging, or disease can erode this perfor-

mance. Mild to moderate hearing loss, corresponding to loss of 20 to 70 dB in tested audibility, can be addressed with external hearing aids. Severe and profound hearing loss, corresponding to loss of more than 70 dB in tested audibility, typically must be addressed with cochlear implants.

A cochlear implant must perform three basic overall tasks. First, it must reduce the dynamic range of sounds to a range that can be managed by the electronics as well as the patient. Second, it has to process these sounds into separate forms for each electrode, ideally to mimic the characteristics of the healthy cochlea. In addition to a microphone input, these sound signals can include electrical feeds or wireless telecoil signals [3]. Third, the implanted unit must stimulate the peripheral nerves of the cochlea with pulses of current. Figure 1-1 shows how the implanted system is configured in the body. The external unit resting behind the ear is a small and highly integrated implementation of cochlear implant design. As miniaturized as this system has become in the past few years, the battery continues to be the largest part of any cochlear implant system.

## 1.2 Cochlear Implant Systems

Figure 1-2 outlines the basic signal processing stages used to make this possible. An automatic gain control (AGC) circuit compresses more than 80dB of audible signal range into 40dB – 60dB depending on the signal processing task or patient preferences. Splitting the signal into multiple channels can be done in many ways. The simplest method is to filter the signal into distinct frequency channels, shown in Figure 1-2 as channel-wise processing blocks. Additional nonlinear compression is needed to map the sound levels into the specific range for each electrode, with levels measured in a post-surgical fitting procedure. Finally the desired stimulation current pulses, often in a particular timing sequence, are sent to the desired electrode.

The total range of currents which will produce the desired effect in patients ranges over a small level – typically no more than 3dB-30dB [4]. In this sense, a broadband AGC stage is accomplishing several necessary and related tasks: By reducing the

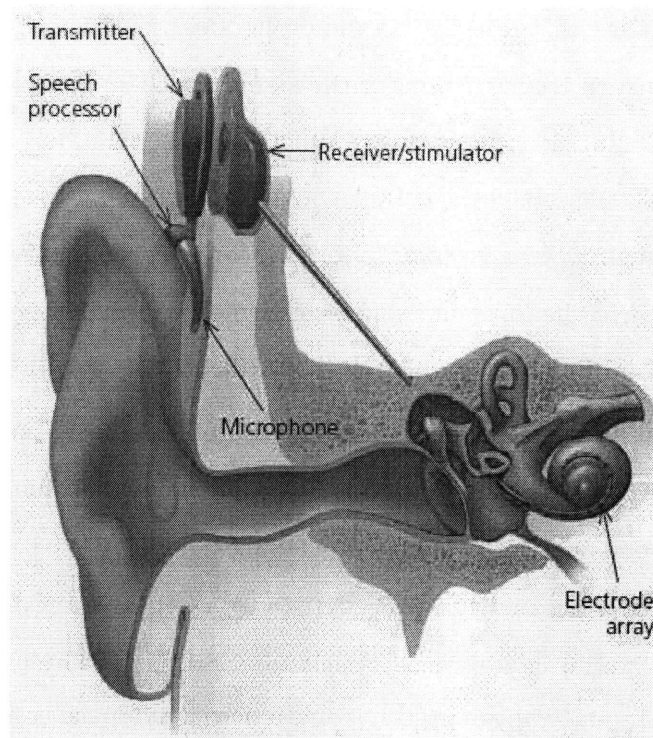


Figure 1-1: A behind-the-ear (BTE) cochlear implant is shown. An external microphone and speech processor process sound signals. A transmitter coil sends power and data into the implanted unit which stimulates the electrode array. Figure used with permission from the National Institute on Deafness and Other Communication Disorders ([www.nidcd.nih.gov](http://www.nidcd.nih.gov)).

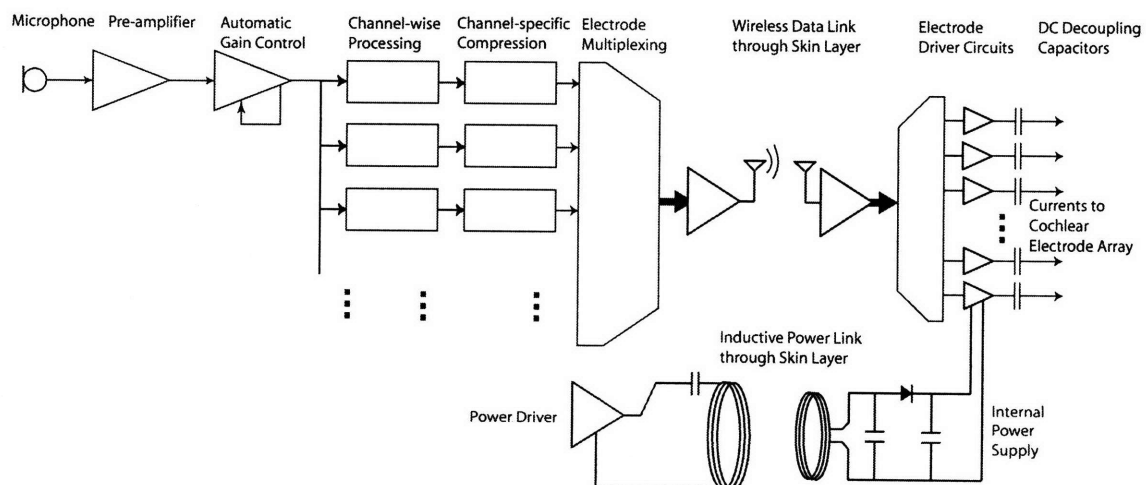


Figure 1-2: The signal processing and power transfer stages in a typical cochlear implant system.

dynamic range of the input signals, the AGC is beginning the process of mapping the wide input signal range to the range of the electrodes. Furthermore, it is adapting the range of signals such that the bulk of the signal processing stages sensitizing the internal channels to soft or loud sounds. Whether these channels are implemented in analog or digital technologies, they can now be low signal-to-noise ratio (SNR) designs, and consequently, lower power [5][6][7]. Moreover, it is providing the patient sound levels adapted to the loud and soft levels which will make sense to the listener – an unsolved problem in hearing research [8][9][10].

Figure 1-2 only tells a small part of the cochlear implant story. Since the electrodes are inside the body and the microphone is outside, the system must be split across the skin at some point along the signal processing chain. A typical implant system will put only the electrode multiplexing, bypass capacitors and electrodes inside the body. This increases the flexibility of signal processing programming because it is external to the body and can be readily replaced without performing surgery. This split also helps simplify the system by requiring that only the stimulation power is sent through the skin, an inefficient process at best [11][12].

Rapid development in cochlear implant technology is being made in many areas simultaneously. Some of these developments are technology driven. For example, flexible signal processing algorithms for the patient have grown with the deployment of programmable digital ASICs [13]. Meanwhile, CMOS technology scaling has reduced the power consumption of these and other front-end blocks reducing battery costs [5][14]. Other advances are driven by better understanding of physiological and neurological considerations. For example, advances in electrode integration are making more sophisticated stimulation possible.

There are, however, many aspects of cochlear implant devices which still require critical improvement. A cost-benefit analysis of cochlear implants finds that implanted individuals benefit greatly from the devices [15]. The personal and institutional costs associated with implants, however, are very high, making them unattractive to many deaf patients. The largest single cost component is the implanted unit itself. In addition to the intensive design and verification that implanted electronics

must undergo, miniaturization of the physical design is the largest contribution of this material cost. Therefore, this thesis will explore the possibility of designing a cochlear implant with reduced power consumption and cost by improving the energy efficiency of signal and power processing stages.

### 1.2.1 Front-End Circuits

Figure 1-3 shows several approaches to the challenge of front ends for generic sound processors. Analog input signals, from a microphone, telecoil, or auxiliary electrical input are first amplified to the appropriate voltage or current level by a preamplifier. Wide-dynamic-range microphone signals can be very small and require low-noise, high-PSRR performance from the preamplifier. Wide-band supply interference is a problem for both analog and digital signal processing systems: In analog systems, the rectification of a corrupted sound signal for envelope detection will mix wide-band interference into the audio range, ruining the sensitivity of the system; In digital systems, aliasing of out-of-band interferers will introduce undesirable tones into the audible range.

Next, an AGC system is needed to reduce the dynamic range before expensive signal processing tasks are performed. The dynamic range level for the processing is referred to as the internal dynamic range (IDR). There are, understandably, several approaches to the task of compressing the microphone dynamic range to the IDR. In hearing instruments this step is particularly critical, since compression of sound signals must be done carefully to avoid uncomfortably loud transients and noise-pumping effects [8][16].

Figure 1-3a indicates an all-digital strategy requiring an A/D converter with wide dynamic range. Figure 1-3b shows an analog AGC followed by a A/D converter only operating on the IDR signal. Finally, Figure 1-3c shows a hybrid approach where the gain-control loop is broken across the analog-digital boundary. Although all of the front end architectures are used in practical applications, each of these approaches has its own benefits and drawbacks. For example, although the all digital system (Figure 1-3a) avoids analog design blocks, improving the reconfigurability of the processing

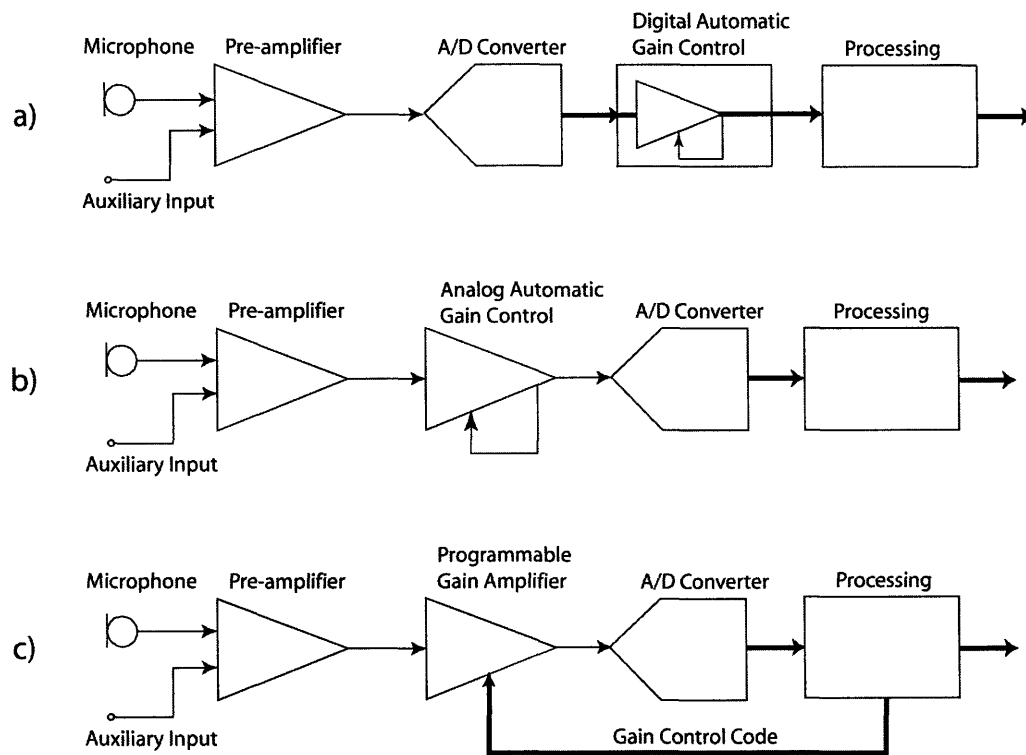


Figure 1-3: Audio front-end architectures with automatic gain control for reducing dynamic range.



scheme, the A/D converter must deal with a wide dynamic range. This can consume a great deal of power [17]. The hybrid system (Figure 1-3c) suffers from having discrete gain levels, which can introduce noticeable transients during slow changes in sound level [5].

This thesis will explore a low-power sense-amplifier design which provides wide-band supply immunity with few external components. Further, this thesis will explore and demonstrate a modular, all-analog, hybrid control AGC architecture for low-power front ends.

### 1.2.2 Power Transfer to the Implanted Stimulator

Powering the implanted stimulator circuits requires transferring energy from outside the body. Advanced cochlear implants have as many as 32 electrode sites stimulating the auditory nerve. As signal processing technology advances, more options are available for low-power design of cochlear implants. Electrode power requirements have only improved slowly with new algorithms and new positioning strategies so electrode power consumption continues to be a large fraction of the total consumption. Thus, delivering power to the implanted unit is not only critical for energy performance of the implant, but also important in reducing the cost of future implants.

Many transcutaneous power systems struggle with obtaining reasonable efficiency [18][19][20]. Where highly integrated power converters can approach efficiencies of 80% – 90%, inductive power links contend with much lower efficiencies, usually in the 30% range [12][21]. While this is partly due to having a number of lossy power processing stages in cascade the inductive link portion of the system requires further understanding. It should be noted that cochlear implant systems must send both data and power into the body requiring the power link to include a data transmission function. Also, back-telemetry data is also often needed to monitor electrode performance, internal supply voltages, and other settings. If designed separately, these systems would use many common parts that increase the size of the design and increase the cost. To deal with these issues current designs have focused on incorporating solutions to both data transfer and power transfer into one design. Many

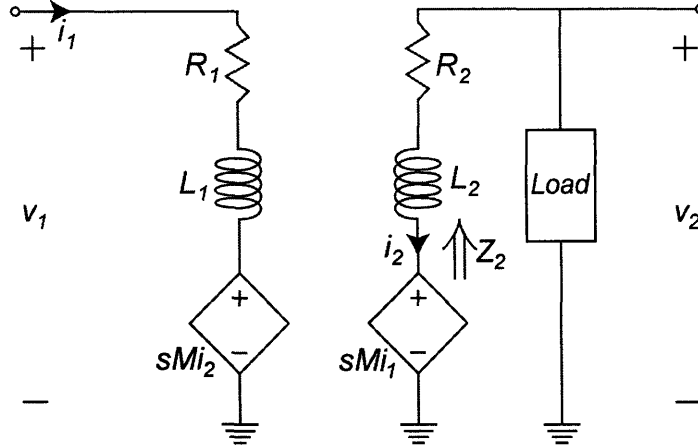


Figure 1-4: The coupling between inductors  $L_1$  and  $L_2$  is modeled as two current dependent voltage sources.

commercial and research designs have successfully incorporated both power and data transmission systems [21][22]. These added features can save board space but can add restrictions to the quality of passive components, the choice of carrier, driver design or modulation scheme.

To design efficient bionic implant systems, a better understanding of the feedback effect between the primary and secondary circuits is needed. Figure 1-4 shows a simple bulk-element electrical model for an inductive link. Resistive losses in the conductors are modeled with the series resistances,  $R_1$  and  $R_2$ . The coupling between the conductors is modeled with current-dependent voltage sources. The mutual inductance term,  $M$ , corresponds to the ratio of the flux linkage between the primary and secondary coils, or  $k\sqrt{L_1 L_2}$ . Loading in the secondary coil appears in the primary coil due to the current dependent feedback.

As coils couple more strongly the impedance reflected from the secondary increases. Without careful considerations for how this effect can reduce the performance, driver efficiency reduces as the coupling increases [12]. This effect is counter-intuitive and merits exploration to benefit inductive link design in general.

This thesis will explore two areas where new strategies are needed. First, a more intuitive model of the inductive link is needed to understand the inductive link deeply. A feedback block diagram model for the elements in the coupled resonator will allow a

simplified perspective and better understanding of the loss mechanisms for the energy transferred across the skin flap.

Second, the design of the power driver must account for changes in the primary circuit impedance and quality factor as the coupling between the resonators changes. To minimize switching losses, power driver circuits must operate with zero-voltage switching. Careful timing, dependent on the load impedances, is required. Control strategies for Class-E and Class-D power drivers utilize fixed delay to predict the timing of power switches.

My driver design will explore the possibility of mitigating the effects of magnetic feedback across the inductive link. Furthermore, a clear understanding of the effect of losses in the passive elements in the inductive link will help to improve the design of inductive power links in general terms and over a broader range of frequencies.

## 1.3 Thesis Outline

Chapter 2 explores the design of current-mode sense amplifier topology suited for a low-power mixed signal environment. Two low-power automatic gain control (AGC) designs are explored in Chapter 3. A simple gain-control algorithm demonstrates the control properties of the continuous feedback case. Next, a more complex state-based hybrid controller addresses patient comfort while building on the robustness of the simple design. Next, the problem of delivering power to an implanted system using coupled resonators is explored in Chapter 4. Chapter 5 discusses an example cochlear implant system using analog and power systems from this thesis. Finally, I summarize my efforts by discussing the role of power-efficient systems in a transcutaneous cochlear implant design and the lessons of this work.



## Chapter 2

# Low-Power Current-mode Microphone Preamplifiers for Mixed-Signal Systems

Modern bionic ears are designed to fit neatly inside the ear, requiring small, low-power, wide-dynamic-range front ends with a minimum of external components and good power supply rejection. The microphone preamplifiers discussed in this chapter<sup>1</sup> address the needs of hearing instruments where low-power and wide-dynamic-range are needed.

The presence of wideband clock and telemetry signals in hearing instruments indicate the need for superb power-supply rejection in-band as well as at high frequencies. A fully analog hearing instrument must exhibit good power-supply rejection properties in all of the stages prior to any nonlinear operation which could introduce mixing of high-frequency noise into the operating frequencies. DSP-based hearing instruments must also have good power supply rejection in the analog front-end to ensure that the A/D is not exposed to mixing and distortion errors caused by high-frequency supply noise.

Wide dynamic range is needed to meet patient needs in noisy environments [2] [23]. Hearing instruments are typically limited to 83dB of input dynamic range by

---

<sup>1</sup>© 2003 IEEE. Reprinted, with permission, from the Journal of Solid State Circuits

available microphone technology. That is, peak signals of 110dBSPL and a microphone noise-floor of 27dBSPL, make most hearing tasks possible. In previous designs, high performance, low power operation, and power supply rejection have required a custom external electret structure [24] [25] [26] [27]. In this work, I show how to obtain high performance specifications with ubiquitous commercial JFET-buffered microphones.

The organization of this chapter is as follows: In Section 2.1, I discuss subminiature microphones. In Section 2.2, I discuss the sense-amplifier topology and its anticipated benefits. In Section 2.3, I discuss designs based on the sense-amplifier approach. In Section 2.4, I discuss experimental results. In Section 2.5, I conclude by summarizing the main contributions of this chapter.

## 2.1 Microphones for Bionic Implants and Hearing Aids

Sub-miniature microphones for hearing aids and cochlear implants are typically self-biased MOS devices buffering the voltage from a moving electret capacitor. The output from the buffer is taken at the source of the MOS device, providing a relatively low-impedance voltage output. Figure 2-1a illustrates the basic microphone circuit showing a depletion-mode MOSFET as the buffer device.

Many manufacturers employ such a self-biased structure to obtain insensitivity to the drain supply voltage,  $V_{DD}$ . The presence of finite output resistance; however, can make the effect of supply noise on the output signal quite pronounced. This problem can be quite serious as many high-frequency signals are present in the implant/hearing-aid environment including carriers for power transfer and communications. Feed-through of high-frequency carriers is problematic when non-linear elements rectify this content to in-band signal frequencies. Figure 2-1b shows a small signal model of the self-biased buffer structure indicating,  $r_O$ , the output resistance of the MOS device as well as its transconductance,  $g_m$ .

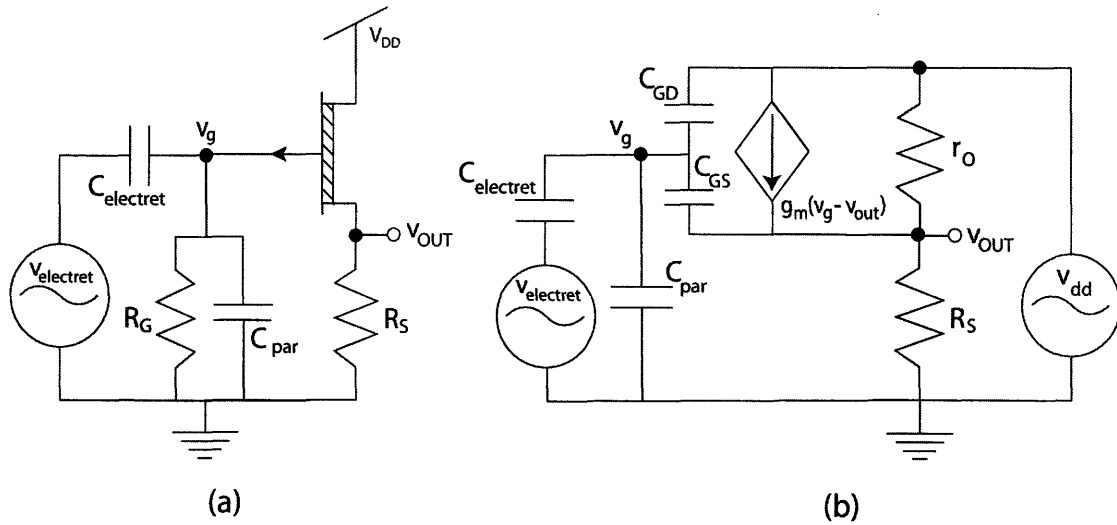


Figure 2-1: Subminiature electret circuit. (a) Low-noise depletion-mode FET device shown with source resistance,  $R_S$ . A large gate resistance is also shown to indicate that the gate is incrementally grounded at low frequency. (b) Small-signal model of the internal structure of the microphone, including the active device and parasitic gate and source resistances.

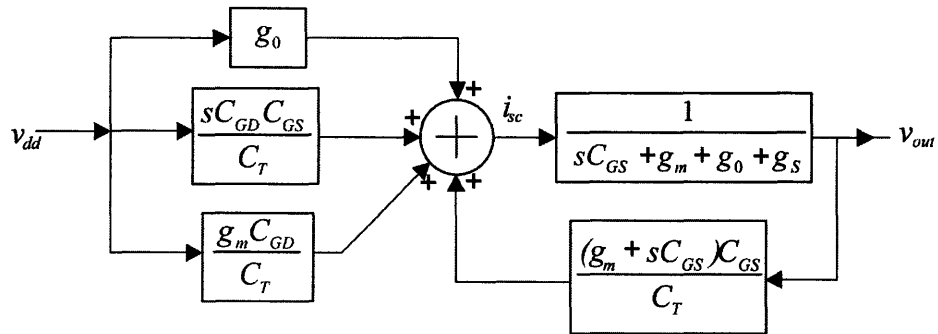


Figure 2-2: Conceptual block diagram of the power-supply noise feedthrough. The summer indicates the summing of currents contributing to the source node of the FET buffer.

The block diagram in Figure 2-2, constructed from the small-signal diagram of Figure 2-1b, shows the contributing mechanisms for power-supply feed-through. The output conductance  $g_0$  and gate capacitances contribute to power-supply tones at  $v_{out}$ . Since the gain of the buffer stage to the transduced electret voltage approaches unity, the power supply rejection ratio of this topology is simply the inverse of the feed-through function. Assuming  $v_{out}$  is grounded, the short-circuit current measured at  $v_{out}$  is due to feed-through from drain-to-source conductance,  $g_0$ , direct capacitive feedthrough, and capacitive-divider and JFET transconductance interaction. These three terms determine  $i_{sc}$ , as shown in Figure 2-2. The output impedance measured at  $v_{out}$  with  $v_{dd}$  and  $v_{in}$  grounded is given by the feedforward block,  $\frac{1}{sC_{GS}+g_m+g_0}$ , if I ignore the  $g_mv_g$  term of the dependent source. Including the  $g_mv_g$  term of the dependent source adds a feedback block from the output with gain  $\frac{sC_{GS}}{C_T}$  as shown in Figure 2-2. Combining all these effects, assuming that  $C_{Electret} \gg C_{GD}, C_{GS}$ , and using Black's formula for feedback loops,

$$\frac{v_{out}}{v_{in}} = \frac{\left(\frac{C_{GD}}{C_T}\right)(sC_{GS} + g_m + g_0)}{sC_{GS} + g_0 + g_m\left(1 + \frac{C_{GS}}{C_T}\right)} \simeq \frac{\left(\frac{C_{GD}}{C_T}\right)(sC_{GS} + g_m)}{sC_{GS} + g_m\left(1 + \frac{C_{GS}}{C_T}\right)} \quad (2.1)$$

where,  $C_T = C_{GS} + C_{GD} + C_{Electret}$ . In many cases, a large FET structure, used to get low-noise operation, results in a large gate-to-drain capacitance. As Equation 2.1 shows, the large gate-to-drain capacitance results in capacitive feed-through of the supply to the output, directly and via the  $g_m$  generator. The challenge of designing high-PSRR front-ends without redesigning the internal structure of modern sub-miniature microphones requires thorough design efforts. While some designs do away with the FET buffer [25], it is clear that this design choice requires manufacturing modifications which are not available to low-cost producers.

The microphone used for this work, a Knowles FG-3329A, has an operating drain voltage range of 0.9 V - 1.6 V and draws  $15\mu A - 30\mu A$  from the supply. The source resistance,  $R_S$ , was measured to be  $20k\Omega$ . Internal gate-to-source and gate-to-drain capacitances were found to be roughly, 80pF and 120pF, respectively, while the electret capacitance was estimated to be 1nF. The measured power supply rejection was



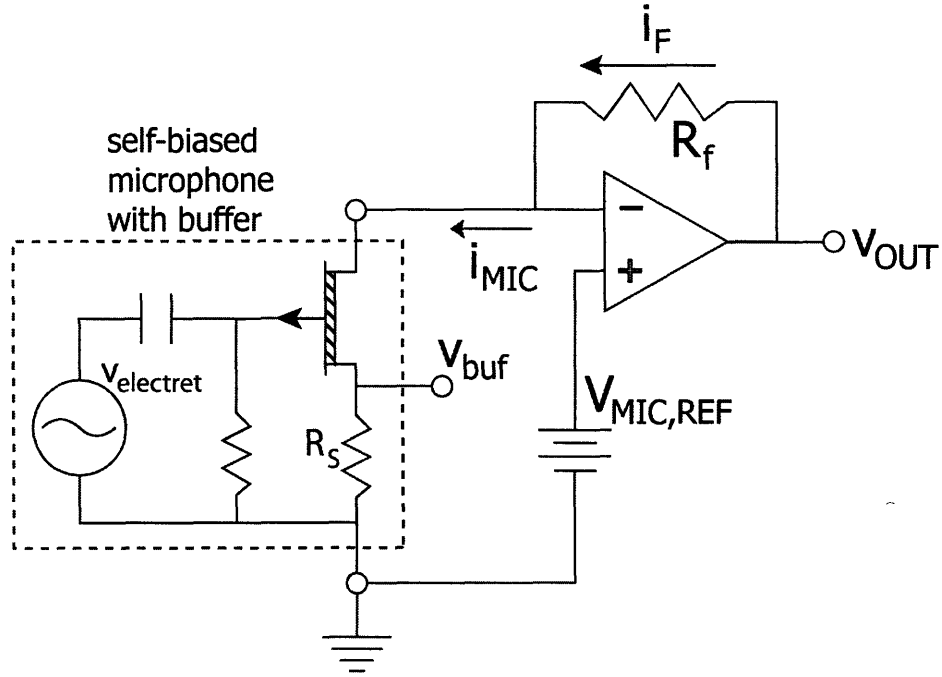


Figure 2-3: A sense amplifier can be used to bias the drain of the buffer JFET as well as provide pre-amplification.

22dB. The total noise from 100Hz to 10kHz is less than  $4\mu V_{rms}$  at the output node,  $v_{OUT}$ .

## 2.2 Sense-Amplifier Topology

A conceptual solution to supply rejection problems is shown in Figure 2-3. A self-biased microphone structure can be configured as the input to a sense amplifier allowing voltage regulation of the drain node. Essentially, I sense the current from the microphone, rather than its voltage, and convert this current to an output voltage through  $R_f$ . The larger the value of  $R_f$ , the larger is the sensitivity of the microphone to sound.

Biasing current for the microphone flows through the feed-back load,  $R_f$ , such that,  $v_{OUT} = V_{MIC,REF} + i_F R_F$ . Referring this new output to the normal output of

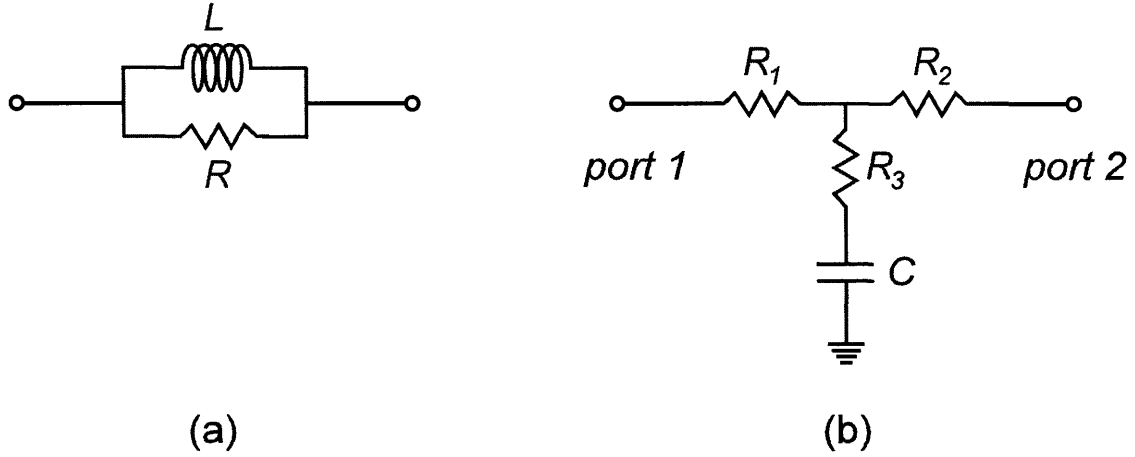


Figure 2-4: Frequency dependent feedback networks are shown which can mitigate the effects of DC current in the feedback path.

the buffer,  $v_{buf}$ ,

$$\frac{v_{out}}{v_{buf}} = \frac{i_{MIC}R_f}{i_{MIC}R_S} = \frac{R_f}{R_S}. \quad (2.2)$$

Front-end gain or sensitivity can be programmed by selecting the feedback impedance,  $R_f$ . More generally, the feedback resistor can be replaced by a two-port network,  $Y_f$ , whose current at the input side and at the output side is a linear function of the voltages at the input and output sides. Since the microphone buffer current is comprised of a large DC component,  $I_{MIC}$ , the the output linear range of the operational amplifier in the sense-amp is degraded by the voltage drop,  $I_{MIC}R_f$ . To make high gain possible while preserving linear range, various two-port networks can be used in place of  $R_f$ . Two choices are detailed in the following section 2.2.1 and shown in Figure 2-4. A practical implementation of these two-port networks imposes performance tradeoffs due to the presence of DC current in the feedback networks.

### 2.2.1 Frequency-Dependent Feedback

Two choices for the two-port network that have good AC gain and that also permits the bias current,  $I_{MIC}$ , to be sourced without taking the op-amp out of its linear DC output operating range are shown in Figure 2-4.

Figure 2-4a shows a choice for the element  $R_f$  which does not sacrifice any output

linear range while maintaining a suitable AC sense-gain of  $R$ . On-chip solutions, however, obviate the use of inductors. On-chip solutions can apply the T-network solution of Figure 2-4b. In the T-network of Figure 2-4b,

$$V_{DC} = I_{MIC} (R_1 + R_2). \quad (2.3)$$

The high-frequency cross-conductance to obtain gain at  $v_{out}$  is calculated by shorting  $C$ , shorting the input port (port 1 in Figure 2-4b), and measuring the short-circuit current at the port as a function of  $v_{out}$ . It is found to be given by,

$$y_{12} = \frac{R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}. \quad (2.4)$$

Conceptually, the T-network network forms a current divider at high-frequencies and attenuates current in the feedback path. Thus, it provides gain at high-frequencies. At low-frequencies, there is no current attenuation, so the DC gain is lower.

A small DC voltage drop from  $v_{OUT}$  to the sense-node at  $V_{MIC,REF}$  is achieved when the total series resistance,  $R_1 + R_2$ , is sufficiently small. Making  $R_3 C$  large yields better gain (larger  $1/y_{12}$ ) at low frequencies. To obtain a high ratio between  $Y_{12}^{DC}$  and  $Y_{12}^{AC}$ ,  $R_3$  is chosen to be much smaller than  $R_1$  or  $R_2$ . At high frequencies, the capacitor,  $C$ , in the shunt branch of the T-network shown in Figure 2-4b is an AC short-circuit. As a result, the driving-point impedance at port 1,  $1/y_{11}$ , is  $R_1 + R_3$  while the driving-point impedance at port 2,  $1/y_{22}$ , is  $R_2 + R_3$ . Since  $R_3$  is small, I may approximate it to be zero when computing the driving-point impedances at either port.

The T-network of Figure 2-4b permits DC current to flow through the feedback element,  $Y_f$ . Thus, I can use the DC current as part of the output stage biasing of the op-amp. Some limitations of this approach become apparent when the requirements on the feedback T-network are reviewed. First, the distortion at the output node,  $v_{OUT}$ , is dominated by the internal signal swing of the op-amp. The gain of the amplifier is set by  $g_{M1}/y_{12}$ , or simply,  $g_{M1}(R_1 + R_3)$ . If the gain of the second op-amp stage is too low, then the swing at the gate, for a given maximum desired

output voltage swing, is large causing distortion. Therefore  $R_1 + R_3$  must be large. Considering the noise performance at the drain of the microphone, the driving point impedance is  $y_{21}$ , or  $R_2 + R_3$ . The current noise contributed to the sense-node from these discrete resistors is,  $\frac{4kT}{R_2 + R_3}$ . To ensure low-noise operation  $R_2 + R_3$  must be large. Consequently, both  $R_1$  and  $R_2$  must be large, making it difficult to satisfy a small voltage drop across the T-network by Eq. 2.3. The dynamic range of this topology is limited due to the conflicting constraints on  $R_1$  and  $R_2$ .

This discussion shows that permitting DC current to flow through the feedback network causes limitations to the dynamic range through both noise and distortion effects. Thus, it is advantageous to have no DC current through the feedback network. I now introduce a split-frequency feedback technique in section 2.2.2 that prevents DC current from flowing through the feedback network.

## 2.2.2 Split-Frequency Feedback

As the microphone bias current only changes slowly with time, a slow feedback loop can be setup to subtract the DC bias current of the microphone without affecting the normal AC operation of the sense-amp. The slow loop then ensures that there is no sensing of the DC current from the microphone while the normal fast sense-amplifier loop transduces the AC current from the microphone into an output AC voltage. Figure 2-5 shows how this approach retains the benefit of my current mode scheme.

Figure 2-5 shows that by driving the DC drop across the sense-amp resistor to zero with feedback, I can subtract the bias current of the microphone and prevent it from causing saturation effects in the operational amplifier. The cancellation of the DC output current can be imperfect without seriously degrading performance. A feedback block diagram indicating both low-frequency and high-frequency loops in Figure 2-5 is shown in Figure 2-6. Because the low-frequency loop can be made arbitrarily slow, its dynamics can be designed so as to not interfere with the high-frequency loop stability. Stabilizing the overall system can then be done without considerations for the performance of the low-frequency biasing loop. It is worth noting that microphone response to unwanted low-frequency vibrations can be reduced through selection of

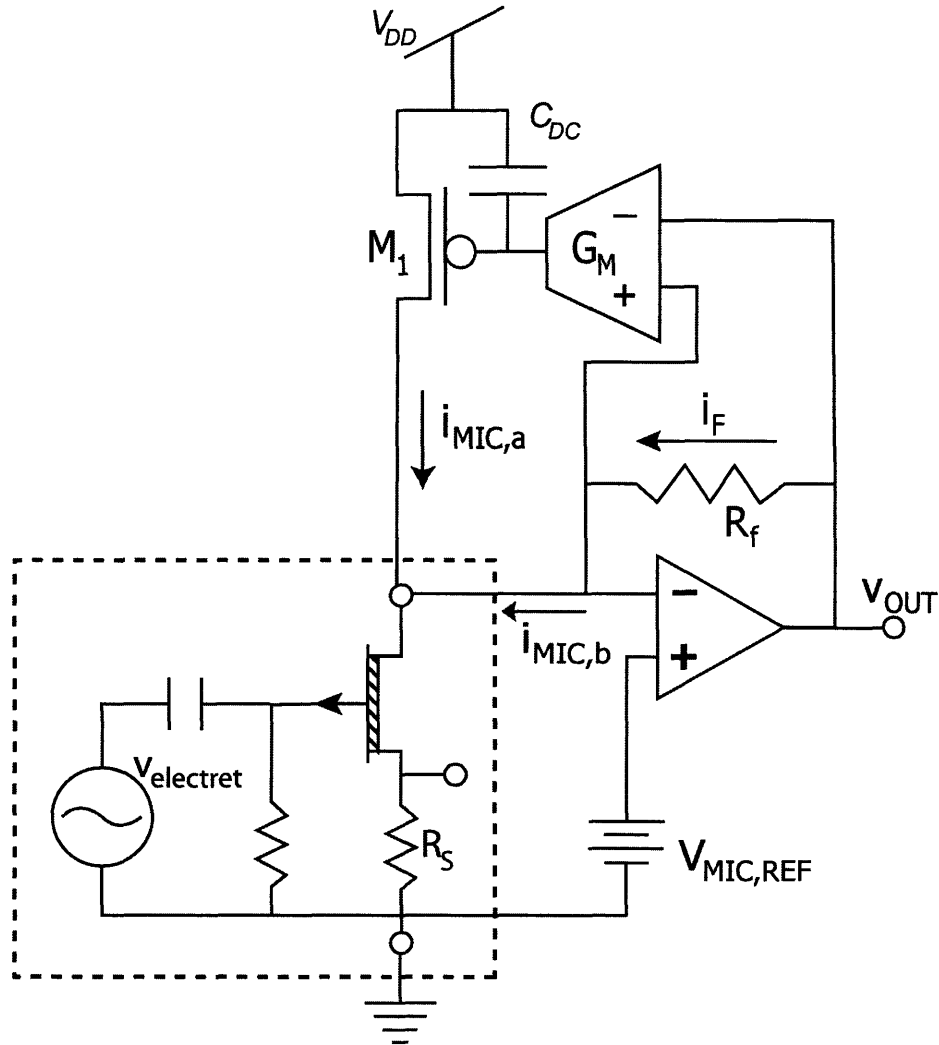


Figure 2-5: Sense amplifier topology employing split-frequency feedback. The DC voltage drop in the feedback load is proportional to the DC output current of the amplifier and is regulated to zero by cancelling the microphone buffer's DC current with feedback DC current from  $M_1$ .

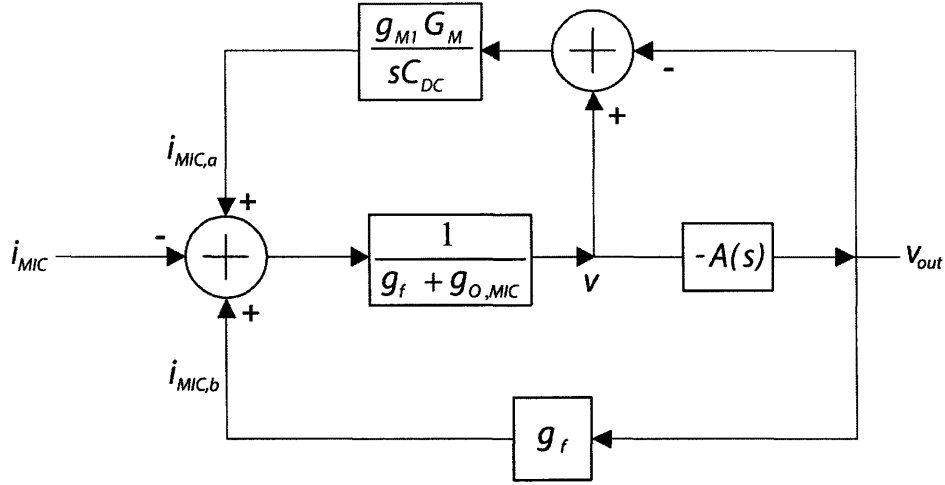


Figure 2-6: Small-signal block diagram for the design presented in Fig. 2-5.

the dynamics of the low-frequency loop.

An additional advantage of this approach lies in the flexibility it affords in the choice of feedback elements. If frequency dependent feedback is to be used, it is no longer required to carry appreciable DC current. If high-pass filtering is desired, a T-network can be used. As no bias current flows through the T-network, the total series resistance in it,  $R_1 + R_2$ , may now be large to ensure low-noise operation, and a small value of  $C$  can still yield a low corner frequency in the filter.

## 2.3 Power-Supply Rejection

For obvious reasons, rejection of power supply noise is a major design constraint for low-noise systems. A variety of non-ideal properties of signal processing systems can contribute to signal degradation. In an all-analog signal processor, rectification and distortion can increase in-band noise drastically through mixing of high-frequency power-supply noise [28]. In digital implementations, power-supply noise picked up at the front-end can result in extensive aliasing in the A/D output. Both of these effects indicate the need for broadband power-supply rejection in the front-end system. While in-band power-supply rejection typically is achieved by employing high-gain feedback, as in our sense-amp topology, such feedback only helps when the

power-supply noise is modeled as an output disturbance that the feedback attenuates. Indeed, past the closed-loop crossover frequency,  $\omega_{CL}$ , noise from the supply is contributed with little attenuation. From this perspective, it is critically important to implement filters to limit the total amount of power-supply noise accumulated in the out-of-band region.

Since in-band power-supply rejection is accomplished with high-gain feedback which I have already implemented with the sense-amp topology, I will focus on filtering of high-frequency supply noise. Several strategies to achieve better noise filtering can be considered. First, we can filter the supply directly, loading the entire supply network with passive elements. These networks are often implemented using inductors to save power. Inductors would be prohibitively large for operation at the frequencies of interest and resistive-and-capacitive filters need to be employed. The DC drop produced in resistive-and-capacitive filters can be minimized by using small resistors. Low cutoff frequencies demand a correspondingly larger capacitor making the filter unsuitable for a small-size solution.

Filtering of high-frequency noise at the output of the analog gain stage, before the A/D conversion, is not without challenges as well. Since the output signal of this stage has been given sufficient gain to drive the full-scale input range of the A/D processing system, it is a significant fraction of the supply range. A filter at this stage would require wide-dynamic range to handle the large output signals.

My approach to power-supply filtering is shown in Figure 2-7a. This figure illustrates how to build a supply-independent current source. The bias device,  $M_1$ , is biased through the large impedance,  $z_A$ , forming a low-pass filter with the gate-source capacitor,  $C_{GS,1}$ . I implement the element  $z_A$  with two parallel diodes with opposite polarity. This strategy yields a DC current source with little response to changes in its source voltage [29].

The power-supply filtering scheme can be analyzed using Figure 2-8 which outlines a block diagram showing a small signal representation of the bias device,  $M_1$ . Effectively, the whole device may be replaced by a small-signal conductance of value

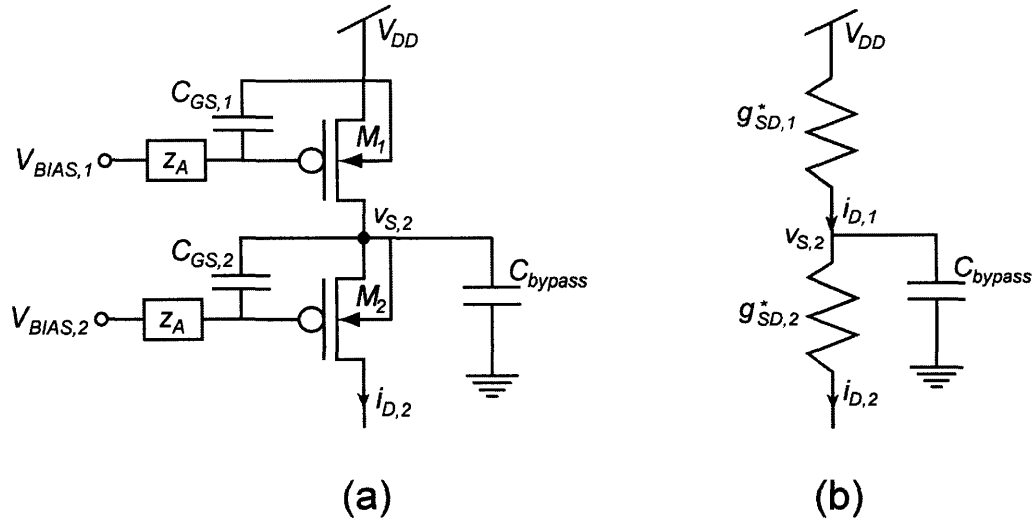


Figure 2-7: Power-supply decoupling mechanism. (a) Explicit gate-source capacitors,  $C_{GS,1}$  and  $C_{GS,2}$ , and biasing of p-gates through high-impedance elements,  $z_A$ , make  $M_1$  and  $M_2$  behave as small-signal large resistances. (b) A bypass capacitor  $C_{bypass}$  filters the supply voltage before it can affect the bias at  $i_{D,2}$ .

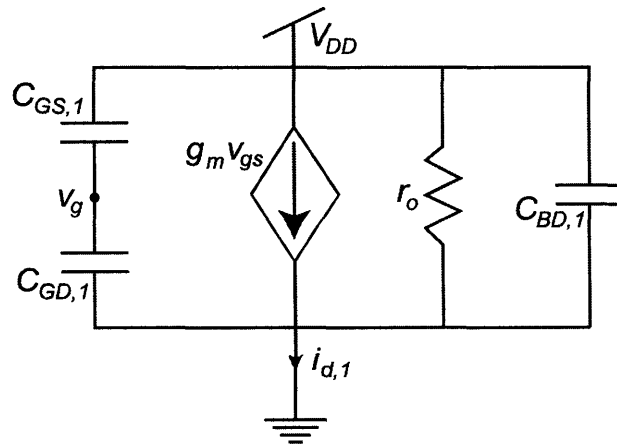


Figure 2-8: Small-signal model of  $M_1$  in Figure 2-7.



$g_{ds,1}$  given by,

$$g_{sd,1} = \frac{i_{d,1}}{v_{dd}} = \left( \frac{C_{GD,1}}{C_{GD,1} + C_{GS,1}} \right) g_{m,1} + g_0 + s \left( C_{BD,1} + \frac{C_{GD,1}C_{GS,1}}{C_{GD,1} + C_{GS,1}} \right). \quad (2.5)$$

As,  $C_{GS,1} \gg C_{GD,1}$ , and  $g_0$  is small, Equation 2.5 can be approximated,

$$g_{sd,1} \simeq \left( \frac{C_{GD,1}}{C_{GD,1} + C_{GS,1}} \right) g_{m,1} + s (C_{BD,1} + C_{GD,1}). \quad (2.6)$$

The drain capacitances of the bias device,  $C_{GD,1}$  and  $C_{BD,1}$ , limit the isolation of output current,  $i_{d,1}$ , from variations in the supply voltage,  $v_{dd}$ . The gate-to-drain capacitance limits the real output impedance of the device by dominating the contribution to  $g_{sd,1}$  over the  $g_0$  term in Equation 2.5 above. Both the gate-to-drain and the bulk-to-drain capacitances contribute to high-frequency feed-through as the last term in Eq. 2.5 and Eq. 2.6 above. Making the gate-to-source capacitance artificially large with an explicit capacitor will help to attenuate the first feed-through term in the RHS of Eq. 2.6. To provide additional filtering, a second device, M2, in parallel with a filter capacitor,  $C_{bypass}$ , can be used to obtain low-pass filtering at the intermediate node,  $v_{s,2}$ . The overall filter characteristic for the output current,  $i_{d,2}$ , can be approximated from Eq. 2.6 and Figure 2-7b. Ignoring the large output resistance,  $r_o$ , and the drain capacitances,  $C_{BD,1}$  and  $C_{GD,1}$ , and approximating  $g_{sd}$  for M1 and M2 as having purely resistive components,

$$g_{sd,1}^* = \frac{C_{GD,1}}{C_{GD,1} + C_{GS,1}} g_{m,1}, \quad (2.7)$$

$$g_{sd,2}^* = \frac{C_{GD,2}}{C_{GD,2} + C_{GS,2}} g_{m,2}. \quad (2.8)$$

The admittance from the supply is,

$$g_{Supply} = \frac{i_{d,2}}{v_{dd}} = \left( \frac{g_{sd,1}^* g_{sd,2}^*}{g_{sd,1}^* + g_{sd,2}^* + s C_{Bypass}} \right) \quad (2.9)$$

The low-pass filtering effect of the bypass capacitor is clear in Eq. 2.9. If the parasitic drain capacitances of both devices are included as,  $C_{D,i} = C_{GD,i} + C_{BD,i}$  (assuming

$C_{GS} \gg C_{GD}$  in Figure 2-8), a limit to the maximum supply rejection is observed from computing the overall supply coupling,

$$g_{Supply} = \frac{i_{d,2}}{v_{dd}} = \frac{(g_{sd,1}^* + sC_{D,1})(g_{sd,2}^* + sC_{D,2})}{g_{sd,1}^* + g_{sd,2}^* + s(C_{D,1} + C_{D,2} + C_{bypass})} \quad (2.10)$$

Two zeros result from the feed-through caused by the drain capacitances. The pole arises from the high-impedance bypass node produced by both p-devices. By choosing  $C_{bypass}$  to be larger than the parasitic drain capacitances, the pole can be made to dominate at lower frequencies, reducing the supply sensitivity at the high-impedance node,  $v_{s,2}$  in Figure 2-7. At frequencies higher than the corner frequency of this filter, the source voltage at the bypass capacitor has limited attenuation from the supply,

$$\frac{v_{s,min}}{v_{dd}} = \frac{C_{GD,1} + C_{BD,1}}{C_{bypass} + C_{GD,1} + C_{GD,2} + C_{BD,1} + C_{BD,2}} \simeq \frac{C_{GD,1} + C_{BD,1}}{C_{bypass}} \quad (2.11)$$

Consequently, it is desirable to make the bypass capacitance as large as possible to ensure the best filtering at high-frequencies.

Due to the presence of a second saturation-region device in the current source of Figure 2-7, its available output voltage range is reduced by my technique. However, supply rejection up to frequencies present in the digital or telemetry system can be achieved if the system supply voltage is not prohibitively low, making my design choice worthwhile. On the 2.8V power-supply, I was able to obtain good power-supply rejection without losing headroom as the experiments in Section 2.4 show.

## 2.4 Experimental Results

My preamplifier and microphone circuitry were fabricated on MOSIS AMI's  $1.5\mu\text{m}$  SCMOS process. Figure 2-9 indicates the two-stage topology of the operational amplifier and the overall pre-amplifier circuit. A 2.8V supply provided power for the circuits and a Knowles Electronics FG-3329 microphone was used. Figure 2-9 also shows the resistive feedback,  $R_f$ , and supply decoupling structures in the drain circuits. The use of supply filters in all supply biasing was found to be critical for high-frequency

rejection performance. The pMOS input stage is comprised of differential-pair transistors M9 and M10, current mirror transistors M11 and M12, and supply-decoupling current-source devices, M1 and M2. Three such current sources are shown. Transistors, M7 and M8 bias the microphone buffer and sense node. The output of the first stage drives M13 in the second output stage. Bypass capacitors were shunted to ground, although another quiet reference could be used. Figure 2-10 shows a die micrograph of the circuits.

The input stage of the operational amplifier was biased at  $6\mu\text{A}$ . The input devices were chosen to obtain a  $1/f$  noise corner near 100Hz. Compensation of the two-stage amplifier was done with the most robust parasitic conditions in mind, i.e. the microphone and auxiliary inputs present capacitive loads to the sense-node, deteriorating the phase margin of the closed loop. Biasing of the second stage was done to ensure load-drive capability for subsequent stages – typically 100pF. Total power consumption for the two-stage amplifier was 34uW. The feedback nOTA was biased with 1 - 3nA while the high-frequency feedback element,  $R_f$ , was chosen around 300k $\Omega$ . The microphone operates at approximately  $20\mu\text{A}$ , adding almost  $60\mu\text{W}$  to the power consumption. Total power consumption was measured at  $94\mu\text{W}$ .

### 2.4.1 Gain

The top curve in Figure 2-11 shows the acoustic gain referenced to the in-band microphone-buffer sensitivity. The FG-3329 has an in-band sensitivity of 17mV per Pascal at the  $v_{buf}$  output in Figure 2-3. Thus, in the top curve of Figure 2-11, a gain of 20dB corresponds to 170mV/pascal. The measured gain was calibrated with respect to a reference microphone in an anechoic environment. The reference microphone and acoustic environment were calibrated Bruel & Kjaer 4232/4188 systems. At frequencies above 10kHz, the flatness of the reference microphone degraded. Consequently the gain calibration exhibits peaks and troughs at high-frequencies.

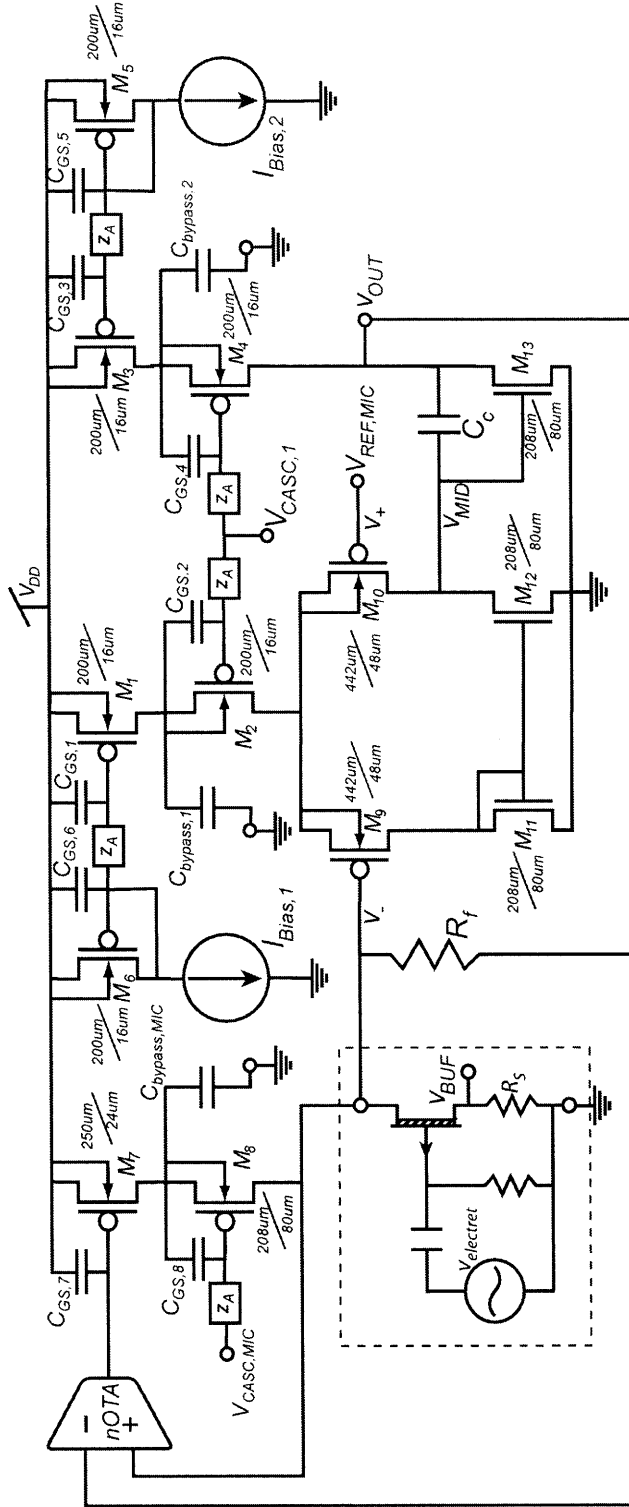


Figure 2-9: Complete circuit topology including the supply decoupling networks. The microphone structure is shown at the bottom left in the dashed box.

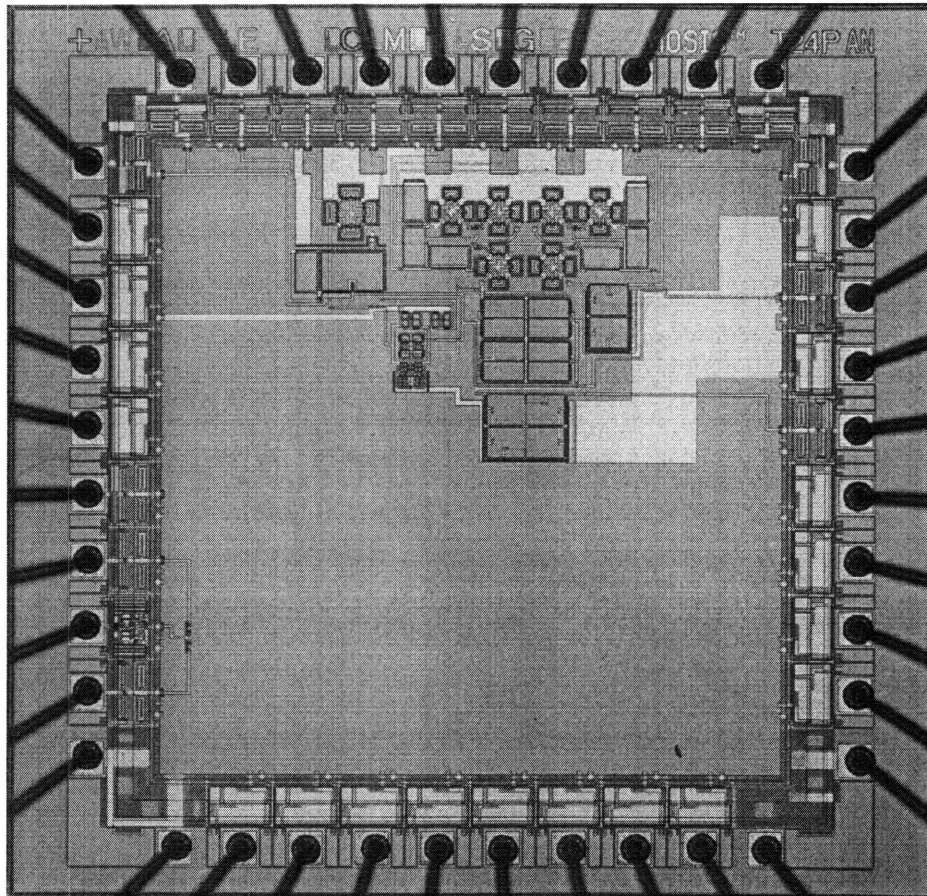


Figure 2-10: Die photo of the current-mode pre-amplifier. The chip is a  $2.2\text{mm} \times 2.2\text{mm}$  chip built in a  $1.5\text{-}\mu\text{m}$  process.

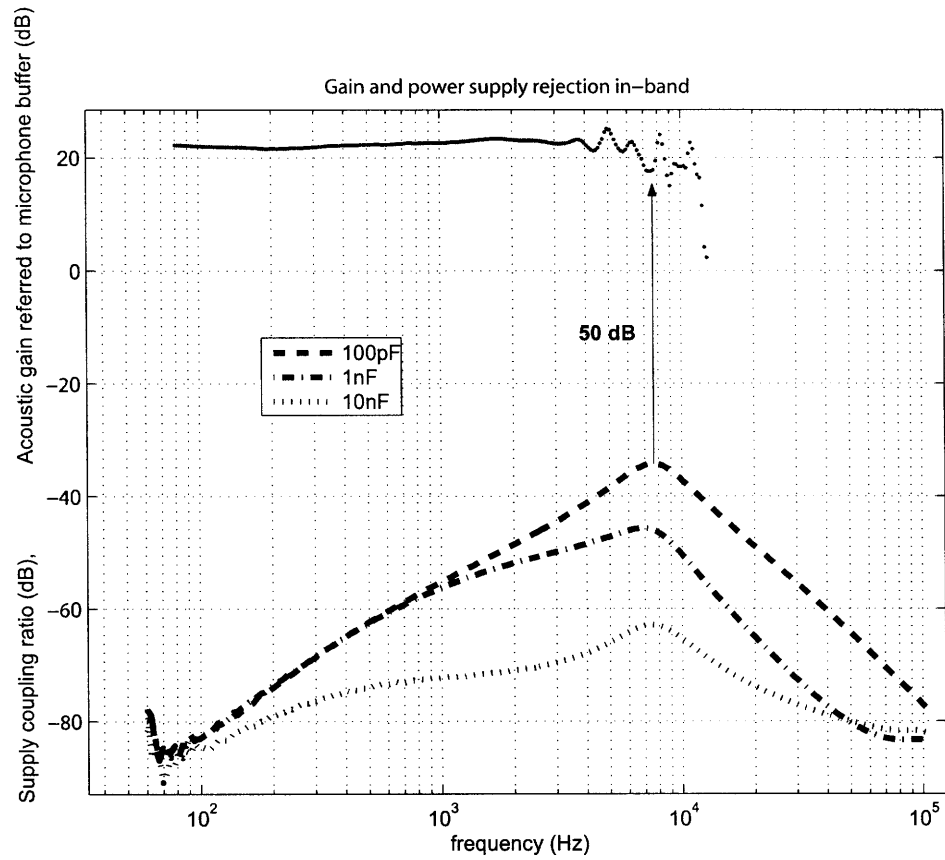


Figure 2-11: Frequency response to acoustic excitation with the output supply coupling response normalized to 1-V<sub>pp</sub> variation of the supply. The supply rejection performance for various bypassing capacitances is shown.

## 2.4.2 Power Supply Rejection

The power supply rejection ratio (PSRR) for the system is the ratio of the voltage gain from  $v_{buf}$  to  $v_{out}$  with respect to the voltage gain from  $v_{dd}$  to  $v_{out}$  in Figure 2-3. Note that  $v_{dd}$  is not explicitly shown in Figure 2-3 but is used to power the operational amplifier. The voltage gain from the supply,  $v_{dd}$ , to the output,  $v_{out}$ , is the sensitivity of the system to supply variations and is shown as the bottom curve of Figure 2-11. The top curve of Figure 2-11 is the voltage gain from  $v_{buf}$  to  $v_{out}$  for the inband audio frequencies. Thus, the PSRR in dB may directly be read off as the difference between the top and bottom curves of Figure 2-11. At 300Hz, 90dB of PSRR is observed, and at 10kHz, 50dB of PSRR is observed. Near 10kHz, the injection of supply noise current excites second-order dynamic behavior in the overall sense-amp producing a peaking effect.

Measurements were made on the system with all bypass capacitances,  $C_{bypass}$ , of value 1nF. To ensure that supply filtering is occurring properly, feed-through data were taken up to 26MHz. This high-frequency rejection data is shown in Figure 2-12. As expected, feed-through effects flatten-out at frequencies higher than the dynamics of the supply filter indicating that the bypass capacitance is dominating the voltage attenuation at the high-impedance filter nodes. Varying the bypass capacitance,  $C_{bypass}$ , changes the attenuation ratio directly, as shown in Figure 2-13. The key factor to note is that potential clock and telemetry frequencies, i.e. greater than 2MHz, are reasonably attenuated even with small capacitances, i.e. with  $C_{bypass}$  of 100pF. A rough estimate of the parasitic drain capacitance,  $C_{pd}$ , contributing to feed-through is estimated at 28fF. Beyond bypass capacitances of 500pF, the coupling to the output does not decrease significantly. This result arises from a static protection resistor built into my chip's pads that limited attenuation.

## 2.4.3 Noise Performance

Figure 2-14 indicates the noise performance of the front-end with and without the microphone contribution. The lower-trace indicates output noise while the microphone

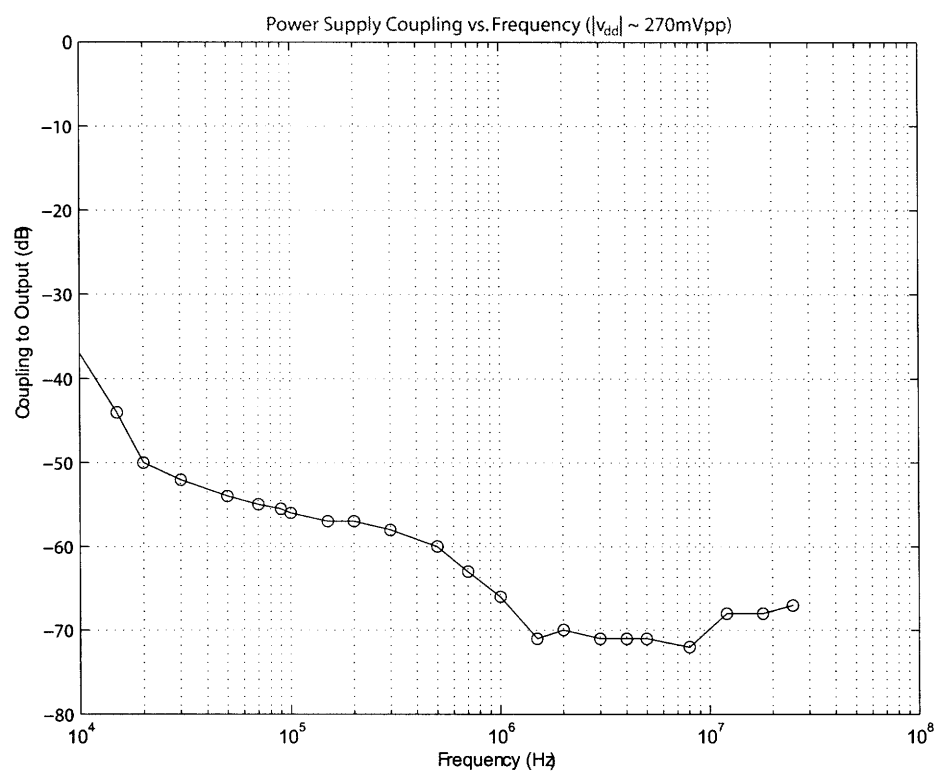


Figure 2-12: Supply coupling for frequencies up to 26MHz.



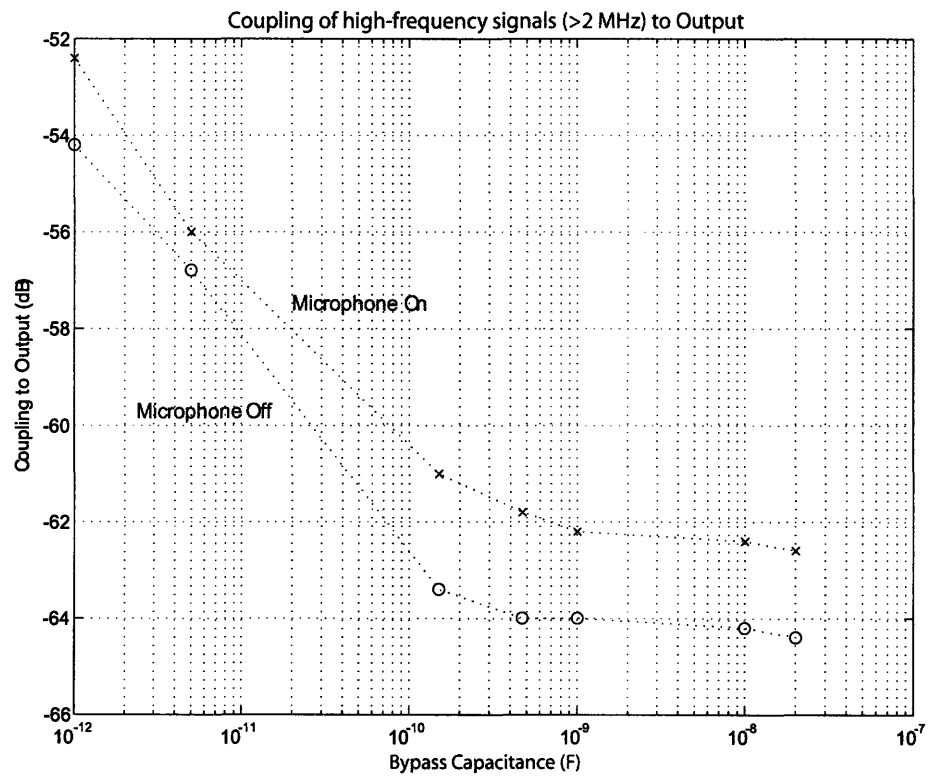


Figure 2-13: High-frequency signals are filtered most effectively from the output in the presence of a large bypass capacitor. A static protection resistor in the chip's pads limited the attenuation of the decoupling path to -64dB.

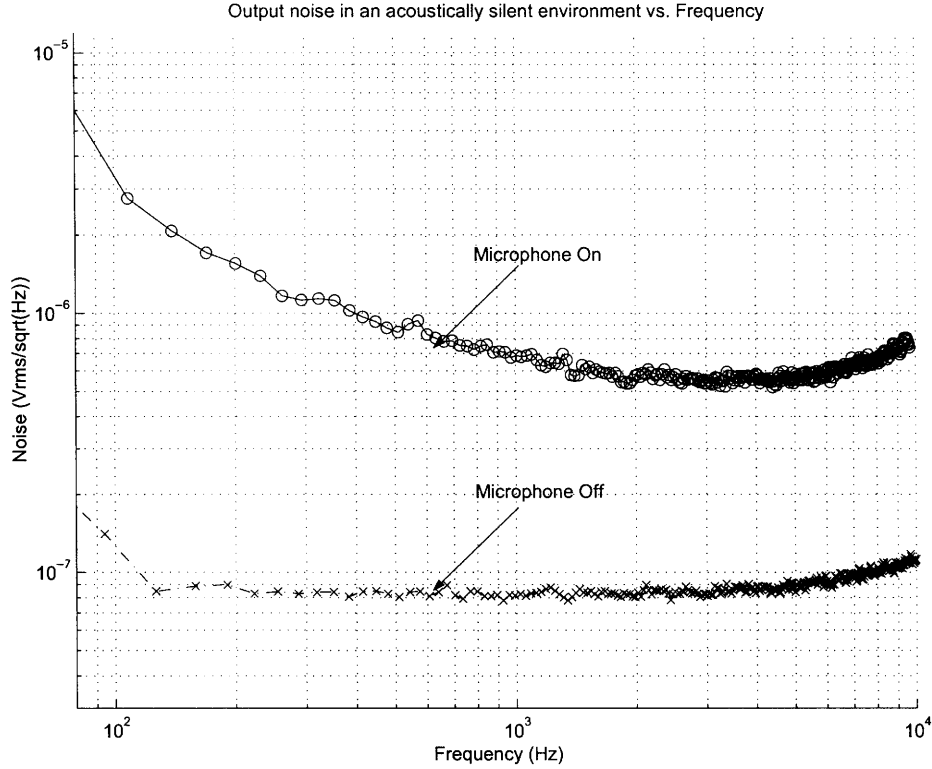


Figure 2-14: Without microphone noise, feedback and operational amplifier contribute  $80\text{--}90\text{ nVrms}/\sqrt{\text{Hz}}$ . The microphone buffer noise dominates when audio input is on. The  $1/f$  nature of the microphone-on characteristic is due in part to the  $1/f$  noise of the DC biasing structure. (Note this figure had a scale error in the published version [30]).

is off. While the microphone is on, the upper trace is obtained. This confirms that the overall noise performance is not limited by the operational amplifier or low-frequency biasing network but by the microphone. Total output noise is  $52\mu\text{Vrms}$  from 100Hz to 10kHz. Referred to the microphone-buffer output/input, this yields an input-referred total noise of  $5\mu\text{Vrms}$  from 100Hz to 10kHz.

An auxiliary voltage-mode input to the sense-amp can be added by sourcing voltage to the sense-node through a resistor,  $R_{AUX}$ . Noise in the presence of this auxiliary channel was also measured. For a voltage-voltage gain of 20dB the total output noise is  $48\mu\text{Vrms}$  from 100Hz to 10kHz for an  $R_{AUX}$  of  $30\text{k}\Omega$ . Referred to the microphone-buffer output/input this noise yields an input-referred total noise of  $4.8\mu\text{Vrms}$  from 100Hz to 10kHz.

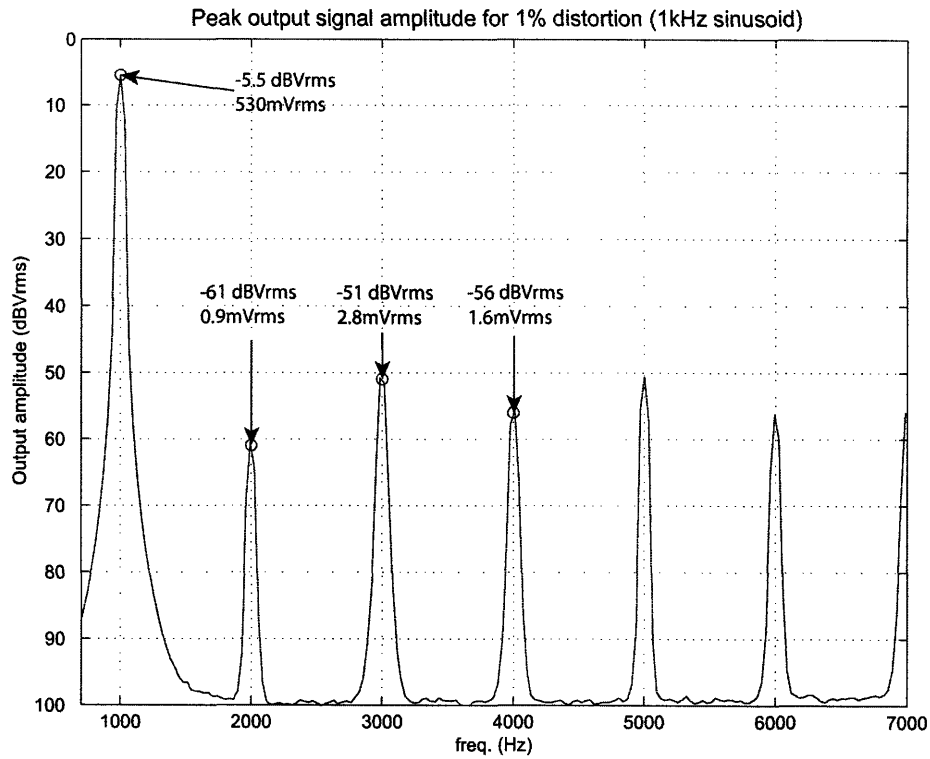


Figure 2-15: Distortion products for 1kHz peak output with 1% distortion.

#### 2.4.4 Linear Range

The output voltage linear range was limited by the power-supply rejection networks. A total harmonic distortion metric of 1% was chosen for best audio performance. A maximum output signal amplitude of 530mVrms was obtained for 100Hz to 3kHz operation with less than 1% distortion. Above 3kHz, second order distortion due to feed-through in the low-frequency bias loop was observed. In Figures 2-15 and 2-16, the transition between the well-behaved distortion characteristics and high-frequency effects are shown. Figure 20 indicates the dynamic range as a function of frequency for the microphone transduction system for 1% distortion limits and a minimum detectable signal of 5 Vrms as a function of frequency. The dynamic range varies from 82dB to 78dB from 100Hz to 10kHz. Both linear range and noise performance are summarized in Tables 2.1 and 2.2.

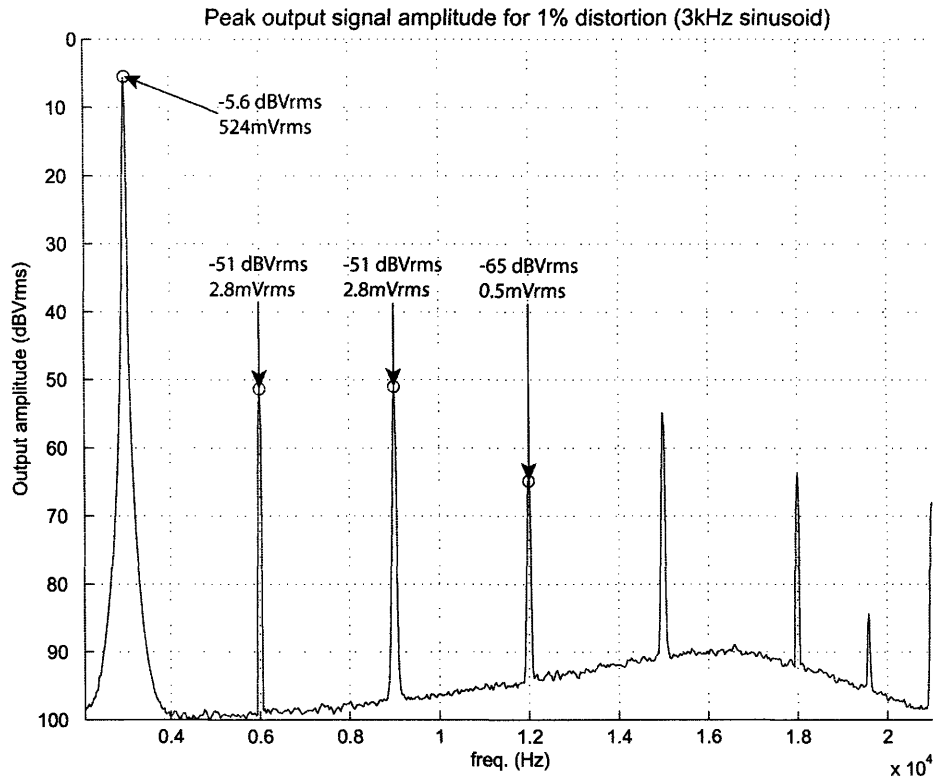


Figure 2-16: Distortion products for 3kHz peak output with 1% distortion.

Table 2.1: Noise and Distortion Performance of Low-Power Microphone Frontend.

Condition	Total Output Noise (100Hz – 10kHz)	Total Input Noise (100Hz – 10kHz)	Output at 1% Distortion	Input at 1% Distortion
Mic: 20dB gain Aux: off	52 $\mu$ Vrms	5 $\mu$ Vrms	530mVrms	52mVrms
Mic: off Aux: 20dB gain	48 $\mu$ Vrms	4.8 $\mu$ Vrms	510mVrms	51mVrms
Mic: 20dB gain Aux: 20dB gain	100 $\mu$ Vrms	10 $\mu$ Vrms	510mVrms	51mVrms

Table 2.2: Overall Specifications for Low-Power Microphone Frontend.

Specification	Measured
Power Consumption	96 $\mu$ W
Dynamic Range at 1% Distortion	80dB
Minimum Detectable Signal	5.2 $\mu$ Vrms (microphone on) 4.8 $\mu$ Vrms (auxiliary on)
PSRR in-band	> 50dB – 90dB
Gain Flatness (auxiliary input)	1dB

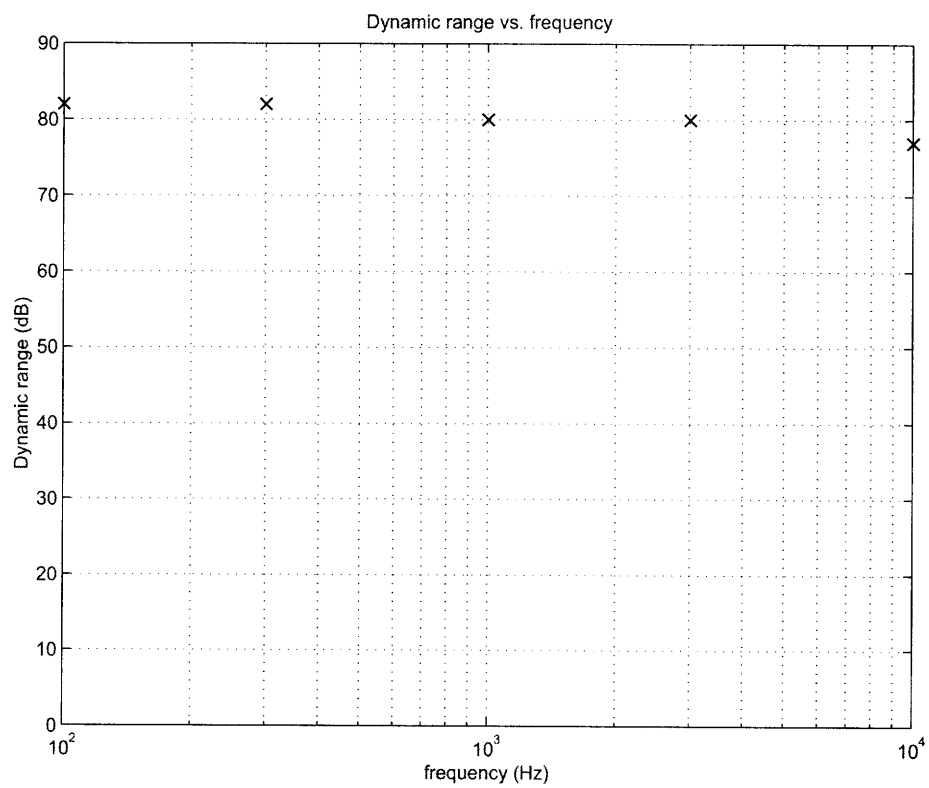


Figure 2-17: Dynamic range versus frequency for acoustic inputs.

## 2.5 Summary

In this chapter, I have demonstrated that a sense amplifier topology is well suited to the task of low-noise supply-immune current-mode amplification of audio signals from both microphones and auxiliary sources. I have achieved wide dynamic range by exploiting the inherent linearity of a sense-amplifier approach and designed bias networks which reduce the effect of noise on supply and bias lines.

Because human hearing sensitivity is frequency dependent, preemphasis filtering can also be desirable for audio inputs. My  $94\mu W$  80dB current-mode sense-amplifier topology can address this need with a frequency dependent feedback network in the place of the feedback resistance,  $R_f$ . The biasing scheme helps make this feasible by eliminating the DC current through the feedback network thus easing the limitations on DC resistance of filter components. This front-end accomplishes the task of amplifying signals from a variety of sources, including possible telecoil attachments, into the hearing prosthesis.

Having designed a front-end for acquiring signals for the hearing instrument I can now turn to the processing of these signals for the cochlear implant. As discussed in Chapter 1 each channel must bandpass filter the signal, followed by a rectifier and asymmetric attack-release filter. To extract the log spectral envelope energy of each channel, a logarithmic A/D operation is performed. If each of these signal processing tasks were to be done on 80dB of precision they would be very costly in power and chip area. We can reduce the amount of precision, required in the channel operations by first extracting the most important information in the signal and operating solely with that precision. Typical speech occurs over a reduced dynamic range – perhaps as little as 40–60 dB. It is possible, therefore, to reduce the precision of the channel processing accordingly. By compressing the speech signal into a smaller output dynamic range, we can drastically reduce the power and area of the channel circuits. At the same time, compression sensitizes these channels to soft and loud sounds as the sound level changes.

In Chapter 3, I will describe how this compression is achieved using a low-power

continuous-feedback automatic gain control (AGC) circuit. There are several challenges in compressing auditory signals. First, an AGC is a nonlinear feedback system, therefore, the stability of such system must be analyzed under several conditions. Second, compressing speech in noisy environments can result in several unintended and unwanted results. Loud transients can be painful for patients when the gain does not adapt quickly enough. To solve both of these problems simultaneously I have designed a smart and low-power AGC system.





## Chapter 3

# Low-Power Single-Loop and Dual-Loop AGCs for Bionic Ears

Wide input dynamic range is needed to meet patient needs in noisy environments. In Chapter 2, I demonstrated a low-power front-end that achieved 80dB of dynamic range. Bionic ears are typically limited to approximately 80dB of unweighted input dynamic range (typically from 30dBSPL to 110dBSPL) by available microphone technology. A broadband AGC between the wide-dynamic-range microphone output, e.g., the one in [31], and the remainder of the processing lowers power and improves sensitivity by reducing the instantaneous dynamic range of operation (IDR) for all spectral channels [2]. An AGC is an example of a compressor since it reduces the wide input dynamic range into a narrower IDR. The IDR is typically somewhere between 40dB to 60dB<sup>1</sup>.

My AGC circuits have primarily been designed for use in bionic ear processors. The circuitry and algorithms for bionic-ear and hearing-aid AGCs, however, are very similar. My AGC circuits can be used as front ends prior to all-analog processing systems for hearing aids, such as those described in [5], or as a front end to subsequent A/D-and-DSP hearing-aid processors. In both cases, power consumption is reduced as a result of the reduced IDR requirements in the processing after the AGC, because of reduced precision requirements in the A/D converter, as well as the analog AGC

---

<sup>1</sup>© 2006 IEEE. Reprinted, with permission, from the Journal of Solid State Circuits.

alleviates the computational burden of the DSP by making a software AGC unnecessary. A charge pump circuit must be used to allow operation at the low supply voltages that are typical in hearing aids. The pump can increase the power consumption by a factor of two to three depending on its efficiency, often limited by parasitics. In this chapter, I will focus on bionic ears but draw on knowledge in the hearing-aid community about AGC design.

Prior work on AGCs has focused on both digital and analog implementations [5][14][24]. In general, digital implementations are capable of complex control, including dual-loop control, and offer maximum flexibility. Analog implementations, however, benefit from all-analog control of the gain variable. First, full-rate and high-precision analog-digital conversion is not required. This adds flexibility and modularity to the design choices in a potential hearing instrument. To make this possible, I implement low-power programmable peak detectors and current-mode decision circuits to support an all-analog gain control architecture. Second, discrete gain levels can interfere with some compression tasks, whereas all-analog approaches preserve the smooth gain transitions during long decays. In this chapter, I describe analog AGCs that implement single-loop and dual-loop control. The parameters of the analog AGCs are programmable via digital bits that alter DAC currents in the system to allow for patient variability.

The organization of this chapter is as follows: In Section 3.1, I review some properties of AGCs relevant to this chapter. In Section 3.2, I discuss my single-loop topology and its properties. In Section 3.3, I discuss the dual-loop control strategy, its anticipated benefits, and relevant circuits. In Section 3.4, I present experimental results. In Section 3.5, I conclude by summarizing the main contributions of this chapter.

## 3.1 Some Properties of AGCs

AGCs are built by having a Variable Gain Amplifier (VGA) vary its gain such that soft sounds are amplified with a large gain while loud sounds are amplified weakly or even

attenuated. If the intensity of the incoming sound changes abruptly, then an AGC will take time to adapt to the new sound level and adjust its gain. Widely used AGCs in bionic ear processors have a single attack time constant for soft-to-loud transitions and a single release time-constant for loud-to-soft transitions and constitute a single-loop AGC. The attack time constant is almost always faster than the release time constant. Slow adaptation results in low distortion to steady-state sounds but sluggish response to transients while fast adaptation can worsen steady-state performance while handling transients better. Compression from 80dB to an IDR below 40dB is usually not advisable in bionic ears. This is because the combination of strong compression and fast time-constants can result in a high level of distortion and discomfort [32]. There is no universal choice of parameters in an AGC that is good for all listening conditions and all input signal statistics, and a compromise is necessary in setting parameters.

Dual-loop control represents a culmination of various efforts to improve performance in conversation and in transient noise environments [33]. Dual-loop strategies have two sets of attack and release time constants, a slow set and a fast set. The slow set adapts relatively slowly to the overall sound level, maximizing listening comfort in the environment, and is usually in use. The faster set is triggered into operation when loud transients are detected, reminiscent of the operation of the stapedial reflex in the human ear. The exact conditions for when slow or fast control are active, the structure of the state machine involved in the decision process, and the state-transition conditions, are described in Section 3.3. Some cochlear-implant patients appear to prefer single-loop AGCs while others prefer dual-loop AGCs, so we chose to implement both kinds of AGCs.

### 3.1.1 Feedforward vs. Feedback Gain Control

AGC circuits can be implemented by sensing the *input envelope* and using it to control the gain of a variable gain amplifier (VGA), according to the desired nonlinear input-output function. Such AGCs are called feedforward AGCs. AGCs may also be built by sensing the *output envelope* and using it to control the gain of the VGA in the

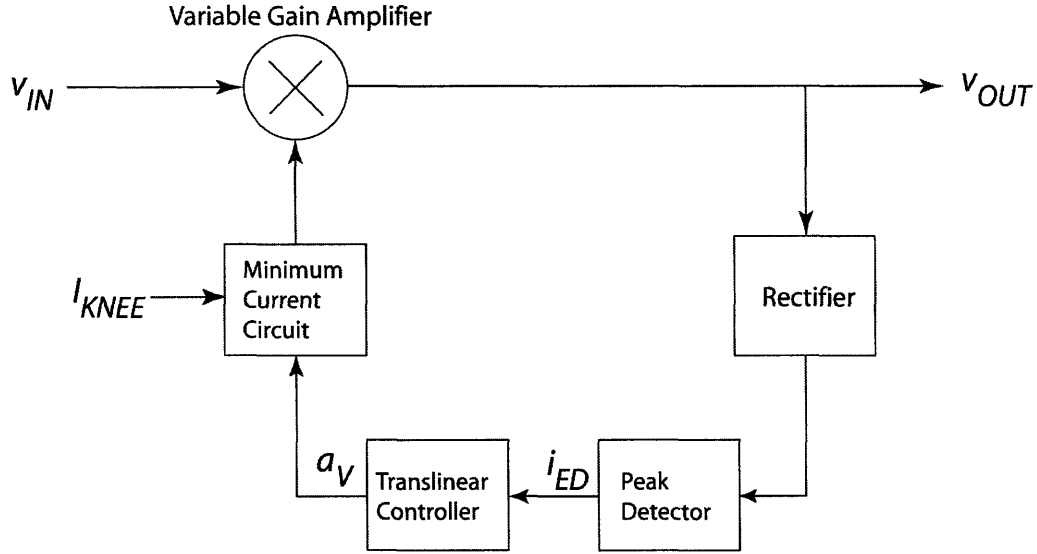


Figure 3-1: Single-loop controller. The envelope signal from the rectifier and peak detector,  $i_{ED}$  and the translinear controller signal,  $i_{GAIN}$ , are shown. A minimum-current circuit enforces a maximum gain by comparing the gain current  $i_{GAIN}$  with  $I_{KNEE}$  and switching the smaller of the two to the VGA.

nonlinear controller, in which case they are called feedback AGCs. There are pros and cons to both strategies as I describe below.

The compression ratio is defined as the ratio of input dynamic range  $DR_{IN}$  to output dynamic range,  $DR_{OUT}$  in dB units, i.e.,  $\frac{DR_{IN}}{DR_{OUT}}$ . The compression ratio for an AGC, which reduces the signal dynamic range, is greater than 1 and, for expansive AGC functions, is less than 1.

Feedforward and feedback controllers must both implement a nonlinear function which satisfies  $CR \times DR_{OUT} = DR_{IN}$ . It is easily shown that, for a feedforward system, the input envelope  $E_{IN}$  should determine the gain  $A_V$  according to

$$A_V = E_{IN}^{\frac{1}{CR}-1} \quad (3.1)$$

The dynamic range of input signals to a compressive circuit is higher than the dynamic range of the output signals. Consequently, sensing the input envelope  $E_{IN}$  in a feedforward topology will require higher circuit performance and more power than sensing the output envelope  $E_{OUT}$  in a feedback topology. The power of envelope

detectors rises proportionately with their required input dynamic range although very wide-dynamic-range and power-efficient envelope detectors have been built [34]. It can be shown that, for a feedback system, the output envelope should determine the gain  $A_V$  according to

$$A_V = \frac{1}{E_{IN}^{CR-1}} \quad (3.2)$$

Equations 3.1 and 3.2 reveal that a feedback controller requires implementation of power law functions of the form  $x^{-(CR-1)}$  while a feedforward controller requires implementation of power law functions of the form  $x^{-(CR-1)/CR}$ . Analog designs of the feedback function are considerably easier to implement than instantiations of the feedforward function especially when  $CR$  is high: For example, if  $CR$  is 5, a feedback topology needs an  $x^{-4}$  function to be implemented while a feedforward topology needs an  $x^{-4/5}$  function to be implemented. A +25% error in the exponent of the  $x^{-4}$  function will change the overall compression from fifth root to sixth root while the same percentage error in the exponent of the  $x^{-4/5}$  function will change the overall compression from fifth root to infinite. Furthermore, the feedback topology attenuates errors in the loop, such as nonidealities in the VGA or disturbances at its output. Feedback topologies, however, are more prone to oscillation and instability and their closed-loop dynamics are a collective function of the dynamics of each open-loop component. In contrast, in feedforward topologies, the dynamics of the overall AGC is simply determined by the dynamics of its nonlinear controller, typically much slower than the dynamics of the rest of the components of the AGC. Nevertheless, I have demonstrated that feedback AGCs show good stability and have dynamics that are relatively level invariant due to the nature of their power-law functions [35]. Taking all these factors into account, I have made a design decision to implement both of my AGCs in a feedback topology for my application.

## 3.2 Single-Loop AGCs

A simple AGC can be realized as in Figure 3-1. A variable gain amplifier (VGA) scales the input,  $v_{IN}$ . The output voltage is converted to a current and rectified. The

rectifier's output current is then filtered by a current-mode filter with a relatively fast attack time-constant,  $\tau_a$ , to increasing changes in input level, and a relatively slow release time-constant,  $\tau_r$ , to decreasing changes in input level. These asymmetric time constants in the filter cause it to function as a peak detector and are programmable with current levels. Output from the current-mode peak detector drives a translinear circuit which decreases the gain current to the VGA as the envelope level of the output signal increases. A minimum-current circuit enforces a maximum gain level by choosing the smaller of the inputs,  $I_{KNEE}$  and  $i_{GAIN}$ .

The rectifier and peak-detector circuits have been described in [34]. The minimum-current circuit, which biases the VGA to the minimum of  $i_{GAIN}$  and  $I_{KNEE}$  has been previously described in [36] and [37]. Therefore, in this chapter, I will focus on the VGA, the translinear controller, and on the functioning of the overall AGC. These circuits are identical in the single-loop and dual-loop AGCs.

### 3.2.1 Variable Gain Amplifier

The variable gain amplifier consists of two wide-linear-range transconductors (WLRs) hooked together in a transconductance-resistance topology. This topology uses an input voltage-to-current transconductor as a current source into a load transconductor. Figure 3-2 shows a circuit diagram of this topology with the voltage-to-current transconductor programmed by the current,  $i_{GAIN}$  and the load transconductor programmed by current,  $I_{REF}$ . The second transconductor, the output WLR, is configured in negative feedback to implement a resistance and is biased with a constant current,  $I_{REF}$ , approximately 100nA. Gain programming is done by changing the  $i_{GAIN}/I_{REF}$  ratio as the transconductance is proportional to  $i_{GAIN}$  while the resistance is proportional to  $1/I_{REF}$ . To keep a fixed bandwidth while the gain is varied, a nearly constant output resistance is required, which is accomplished by keeping  $I_{REF}$  fixed. Thus, Figure 3-2 shows how I have implemented the programmable VGA with transconductors.

One of the WLRs from Figure 3-2 is detailed in Figure 3-3. To improve the linear range of the input differential pairs, the input voltages drive the well nodes in the

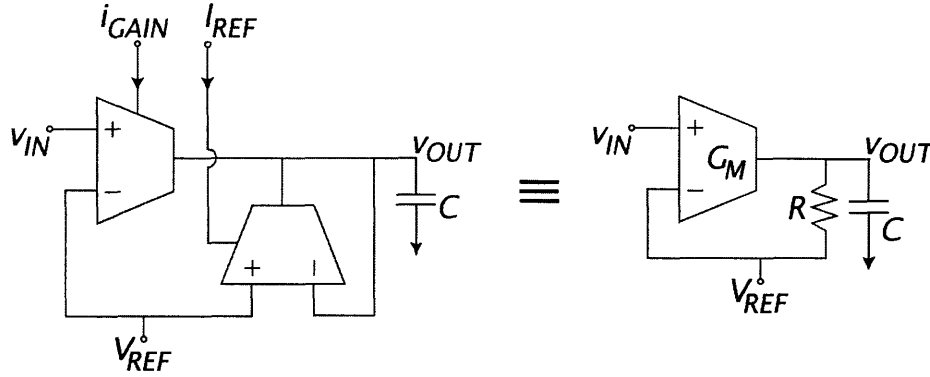


Figure 3-2: VGA block diagram. The ratio of currents  $i_{GAIN}$  and  $I_{REF}$  in the input and output amplifiers, respectively, determine the gain of the circuit. The reference current level  $I_{REF}$  is usually about 100nA, and the gain current  $i_{GAIN}$  is usually from 100nA – 1.2 $\mu$ A.

input transistors  $M_1$ ,  $M_2$  rather than their gate nodes, due to their lowered transconductance for a given current [38]. Each input transistor has its transconductance lowered further through a technique called *gate degeneration*: Increases in current in the arm of the differential pair in which the transistor belongs causes a voltage drop on a diode ( $M_2$  in Figure 3-3). This drop is fed back to the gate of  $M_2$  in the diff-pair transistor to turn it off. This strategy, called gate-degeneration [38], increases the linear range by lowering the transconductance, using feedback in a manner analogous to source degeneration where increases in current in diff-pair transistors are fed back to the source to reduce it. The devices  $M_3$  and  $M_4$  steal the tail current of the differential pair at low differential voltages and return it at high differential voltages such that the compressive saturating nonlinearity of the differential pair is linearized by an expansive tail-current nonlinearity in this technique, called *bump linearization* [38]. The common-mode operating point of the circuit must be chosen to be sufficiently high, typically more than 0.8V at low bias currents, to avoid turning on the well-to-source node in the well-input transistors. The net linear range of such a transconductor in this process is then nearly 1V for subthreshold bias currents instead of 75mV for a simple differential pair.

Distortion in the VGA can be caused by large inputs to the differential pair of

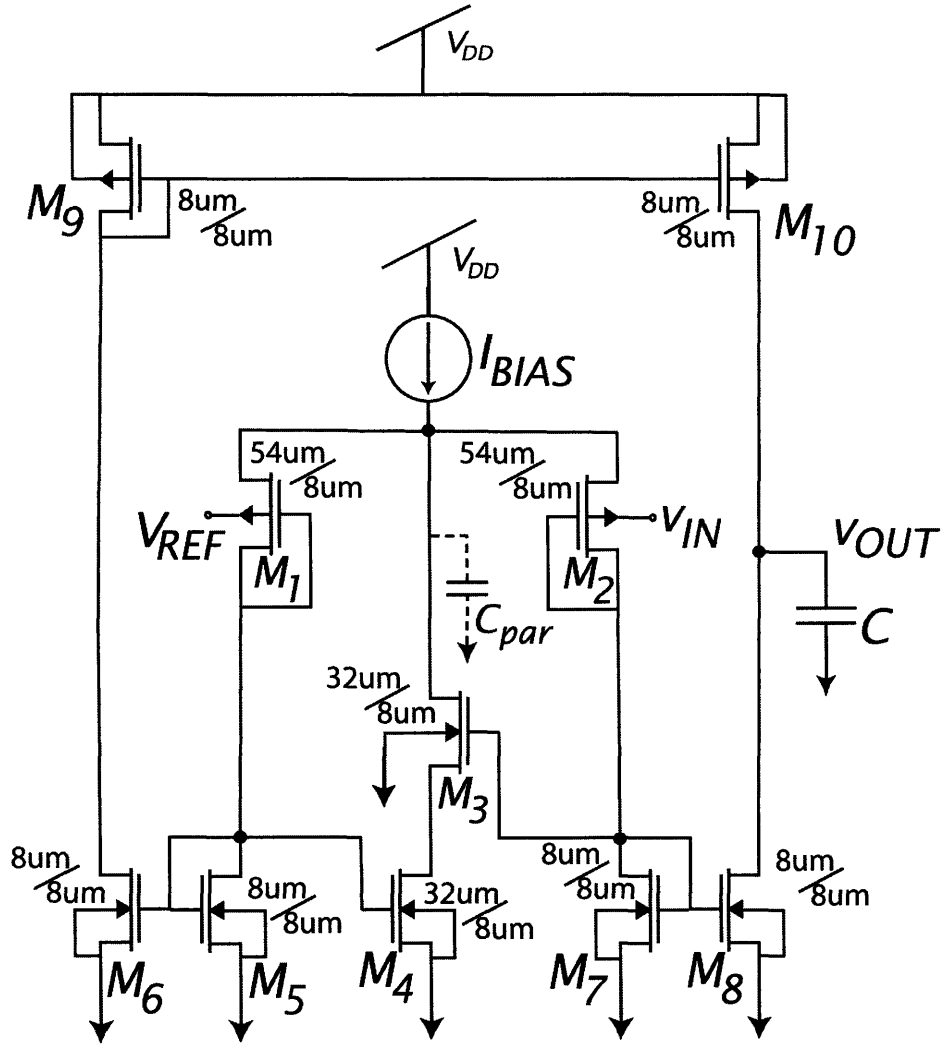


Figure 3-3: One of the transconductors from the VGA circuit. The transconductor uses wide-linear-range circuit techniques – bulk inputs, gate-degeneration, and bump linearization described in the text [38].



the input WLR stage or by large inputs to the differential pair of the output WLR stage. If either transconductor has differential inputs that are comparable to its linear range, distortion is increased. When the input signal is small, the input stage has little differential input and does not distort the signal significantly; however, the gain is high such that the output stage contributes most of the distortion, although this distortion is usually quite small. When the input signal is large, the input stage dominates the distortion [39].

Low noise in the VGA is necessary for a large instantaneous dynamic range of operation or instantaneous output signal-to-noise ratio ( $SNR_{OUT}$ ), an important requirement for faithfully capturing transients. Since the AGC is mostly operated with subthreshold bias currents, the contribution of  $1/f$  noise may be neglected to first-order approximation, as has been shown previously [40]. The reason that  $1/f$  noise may be neglected in subthreshold to first approximation is that the input-referred thermal noise levels are extremely high due to the low transconductance and power levels of devices. As experimental and theoretical measurements in [39] show,  $1/f$  noise becomes more significant only at current levels that are in strong inversion, moderate inversion and relatively high subthreshold current levels.

As I show later, my experimental measurements in this chapter confirm that this approximation is a good one. If white noise dominates, the input-referred noise of the VGA lowers as its bias current and gain increases, while its output noise increases. This behavior is caused by the fact that the input noise in a fixed bandwidth system such as this is inversely proportional to the transconductance of transistors in the WLRs. The output noise is directly proportional to the transconductance of these same devices. Assuming that each WLR contributes  $N$  devices worth of white noise, and that a bias current of  $I_{GAIN}/2$  and  $I_{REF}/2$  flow in each device of the WLRs respectively, it is easy to show that the net output current noise per unit bandwidth due to the noise of all the devices is given by classic shot-noise-like formulas for white noise in subthreshold [38][40] to be

$$\frac{i_{nz}^2}{Hz} = 2q \left( \frac{I_{GAIN}}{2} + \frac{I_{REF}}{2} \right) N, \quad (3.3)$$

where,  $q$  is the charge on the electron,  $1.60217 \times 10^{-19}C$ . This noise is converted to an output voltage noise by multiplying by the resistance of the output WLR,  $V_L/I_{REF}$ , to get

$$\frac{v_{nz}^2}{Hz} = 2q \left( \frac{I_{GAIN}}{2} + \frac{I_{REF}}{2} \right) N \frac{V_L^2}{I_{REF}^2}, \quad (3.4)$$

where  $V_L$  is the peak voltage swing (i.e. half of the peak-to-peak voltage swing) linear range of the WLRs. This noise per unit bandwidth is integrated over the equivalent noise bandwidth  $f_{ns}$  of a single-pole lowpass filter given by

$$f_{ns} = \left( \frac{1}{2\pi} \right) \left( \frac{\pi}{2} \right) \left( \frac{I_{REF}}{CV_L} \right), \quad (3.5)$$

where,  $C$  is the output capacitance in Figure 3-2. The  $\pi/2$  factor accounts for excess noise in a non-rectangular lowpass filter, and the  $(1/2\pi)$  factor converts from angular frequency to regular frequency. If I multiply Equation 3.4 by the bandwidth of Equation 3.5, using the gain of the AGC,  $A_V = I_{GAIN}/I_{REF}$ , and do the algebra, I get,

$$v_{nz,TOTAL} = \sqrt{\frac{qN(A_V + 1)V_L}{4C}}. \quad (3.6)$$

In this form, I can compute the output signal-to-noise ratio ( $SNR_{OUT}$ ) as a function of the gain by writing,

$$SNR_{OUT} = \frac{v_{OUT,MAX}^2}{v_{nz,TOTAL}^2}, \quad (3.7)$$

where  $v_{OUT,MAX}$  is the maximum relatively undistorted signal that I am willing to tolerate. If I assume that this is set by the linear range of the transconductors to be  $V_L$  [38] such that the maximum signal has RMS energy of  $(V_L^2/2)$ , then,

$$SNR_{OUT} = \frac{2CV_L}{Nq(A_V + 1)}. \quad (3.8)$$

In this analysis, I have neglected contributions to the output noise caused by variations in the gain  $A_V$ . Such variations are due to noise in the rectifier, peak detector, translinear controller, and minimum-gain circuit. Such noise contributions were intentionally minimized in this AGC through the use of a large capacitance,  $C_T$ , at the

output of the translinear feedback network and filtering in these circuits. If I include such noise sources, then Equation 3.8 would need to be modified to read,

$$\frac{1}{SNR_{OUT}^2} = \frac{qN(A_V + 1)}{2CV_L} + \frac{\Delta A_V^2}{A_V^2}, \quad (3.9)$$

where the added term reflects variations in the gain  $A_V$ .

The total output load capacitance,  $C$ , due to loading by the envelope detector and an output buffer is approximately 3pF. To maintain 10-kHz bandwidth, the minimum  $I_{REF}$  current that can be used is nearly 100nA. The linear range of the WLRs is near 1V. The number of noise sources from each WLR can be shown by a noise analysis similar to that in [38] to be approximately 5. Since  $A_V$  varies from 1 to 12 in my application, my  $SNR_{OUT}$  from Equation 3.8 in dB units is predicted to vary from 65.7dB to 57.6dB as  $A_V$  increases. I will later show that the experimental measurements are in good accord with this theoretical prediction.

At any given fixed value of  $A_V$ , the AGC may be viewed as a linear system that scales its input by  $A_V$  to create its output. Consequently, the range of input signal strengths over which  $SNR_{OUT}$  is always greater than 1 and over which the distortion is tolerable, i.e., its instantaneous dynamic range (IDR), can be computed by simply dividing the numerator and denominator of the right hand side of Equation 3.8 by the constant  $A_V$ . Equation 3.8 also yields the IDR over which transients will be faithfully reproduced. For signal strengths outside this range, the AGC will need to adapt and adjust its gain over a settling time determined by its dynamics before it can faithfully reproduce them. Thus, rapidly changing signals outside this range will either be buried in the noise or distorted during the adaptation time of the AGC. A well-designed AGC will have an IDR large enough to capture most transients in the signal statistics and be agile enough to change its gain over time as the long-term input signal statistics change. My AGC fulfills these requirements for bionic ears since the instantaneous dynamic range of speech is rarely above 35dB, and talker effort, talker variability, and talker distance rarely increase the instantaneous required dynamic range to more than 55dB. The IDR required for bionic ear applications is usually in

the 40dB to 55dB range.

A variety of distortion mechanisms contribute in the VGA: Variations in the depletion capacitance of the MOSFET caused by modulating the well inputs of the WLRs produce second-order distortion that dominates the VGA. Other distortion mechanisms, including slewing at internal nodes and at the output node, also contribute a little.

### 3.2.2 Translinear Circuit Design

Implementing the control equation necessary for my AGC,

$$I_{GAIN} = K \left( \frac{E_{REF}}{E_{OUT}} \right)^{CR-1}, \quad (3.10)$$

is equivalent to implementing the equation,

$$\log I_{GAIN} = \log K + (CR - 1) [\log E_{REF} - \log E_{OUT}], \quad (3.11)$$

in the logarithmic domain. Here,  $E_{OUT}$  corresponds to the output envelope of the AGC,  $CR$  is the compression ratio, and  $E_{REF}$  is a reference envelope at which the controller's output is determined by  $K$  and is independent of the compression ratio. Figure 3-4 shows an implementation of the latter equation with bipolar transistors, linear transconductance amplifiers, and a final exponentiation in the transistor Q4 to obtain  $I_{GAIN}$ . It is easy to show through simple translinear circuit analysis that the overall circuit implements the equation,

$$i_{GAIN} = I_{REF} \left( \frac{I_{EDRef}}{i_{ED}} \right)^{(G_1/G_2)}, \quad (3.12)$$

such that Equation 3.12 is analogous to Equation 3.10 with  $CR$  given by  $(1 + G_1/G_2)$ . The current  $I_{EDRef}$ , is chosen as the highest current which can be sourced from the envelope/peak detector circuits for linear operation of the VGA. This ensures that when the envelope detector output current,  $i_{ED}$ , corresponds to the maximum output amplitude, no current is sourced from  $G_1$  and that  $i_{GAIN}$  is independent of the  $G_1$

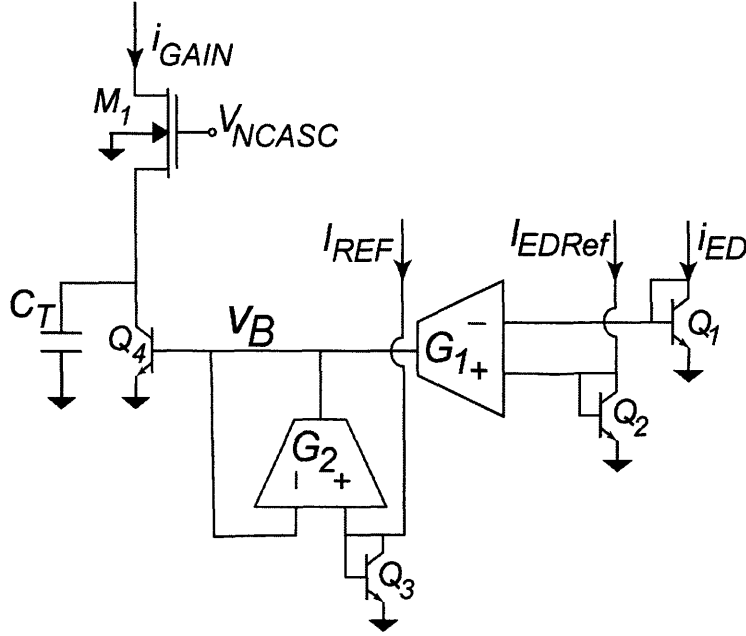


Figure 3-4: A translinear circuit implementing an inverse exponential is computed using a pseudo-linear voltage divider. The voltage divider sums the influence of the logarithm of the envelope current,  $i_{ED}$ , with the reference current,  $I_{REF}$ . Bipolar transistors are used to avoid above-threshold effects in MOS devices. A filter comprising a capacitor  $C_T$  and an nMOS cascode transistor  $M_1$  is included at the output node.

or  $G_2$  and only dependent on  $I_{REF}$ . This independence allows us to decouple the rectifier-and-peak detector current levels from the VGA's current levels and to greatly simplify the programming of the AGC. The maximum gain of the AGC then becomes independent of the compression ratio and is set by  $I_{REF}$ . In my AGC, this is one since  $A_V = i_{GAIN}/I_{REF}$  is 1, when  $i_{GAIN} = I_{REF}$ .

To simplify subsequent equations, the exponent in Equation 3.12 will be called the compression factor and abbreviated as  $\alpha = G_1/G_2$ . The relation of this compression factor to the compression ratio is given by  $\alpha = CR - 1$ . When the compression ratio is one, the ratio of envelope and reference currents has no effect on the operation of the VGA, since I now have a linear system with constant gain.

The output transistor, Q4, is cascoded by transistor M1 and combined with  $C_T$  to create a lowpass filter. By making  $C_T$  large, we can limit fluctuations in the total gain  $A_V$ . The capacitor,  $C_T$ , is an onchip capacitor of approximately 150pF

implemented with MOS capacitors to minimize chip area. The values of  $i_{GAIN}$  are still large enough in the AGC such that the additional time constant created by this filter does not affect the loop dynamics greatly since the envelope-detector dynamics are extremely slow and dominate the loop's performance.

### 3.2.3 Translinear Circuit Offsets

My discussion of the output current so far ignores the offsets in the circuit elements of Figure 3-4. If I absorb all circuit offsets into an equivalent offset at the input of transconductor 1,  $V_{OFF1}$ , and an equivalent offset at the input of transconductor 2,  $V_{OFF2}$ , I can show that Equation 3.12 is given by,

$$I_{GAIN} = I_{REF} \left( \frac{I_{EDRef}}{I_{ED}} \right)^\alpha \left[ e^{(\alpha V_{OFF1} - V_{OFF2})/\phi_t} \right]. \quad (3.13)$$

Both transconductors in the circuit must accommodate voltage ranges on the bipolar base-to-emitter voltages corresponding to as much as 80dB of dynamic range. Thus, each of these transconductors was designed to have more than 240mV of input linear range as base-to-emitter voltages increase by 60mV for every 20dB increase in current. Since  $I_{KNEE}$  is a subthreshold current and requires digital calibration, I provide four bits of correction that allows it to be adjusted in the  $100nA - 1.1\mu A$  range. Assuming a typical 3% offset in both transconductor's input voltages, I can compute a worst-case error in the gain current,  $i_{GAIN}$ , of 75%. Since the error is exponentially dependent on these offsets, it is critical to have well-matched input stages for these amplifiers and generate the bias currents using techniques robust to temperature variations [36][41]. In my AGC, when the maximum signal is present, the value of  $i_{GAIN}$  is typically in moderate inversion and shows relatively good matching with design. I can thus effectively compensate for these offsets in a feedforward fashion.

### 3.2.4 Log-Linear Controller Properties

Log-linear AGC loops based on equations like those of Equation 3.10 have been studied in early work on gain control [10]. One of the key benefits of such AGC loops

is that they exhibit internally nonlinear but externally linear dynamics. Remarkably, in spite of the logarithmic nonlinearities of the translinear controller and the multiplicative nonlinearity of the VGA, the system dynamics are independent of the signal level. Linear feedback analysis provides insight into such operation and can be applied to create a linearized version of the feedback loop of Figure 3-1.

Assuming that the peak-detector filter responds slowly and with little ripple, I can rewrite the AGC loop in terms of the envelopes of its input and output signals  $e_{IN}$  and  $e_{OUT}$ . For each element of the loop, a linear small-signal equivalent can be derived as a function of the DC operating points,  $E_{IN}$  and  $E_{OUT}$  just as in standard small-signal circuit analysis. The envelope detector and peak-detector blocks are approximated with a transconductance gain of  $G_{ED}$  and a time constant of  $\tau_a$ . The multiplier element is easily linearized by noticing the influence of both the control and input envelope signals on the output envelope signal. By the small-signal definition,

$$\left. \frac{\delta}{\delta e_{in}} (e_{in} \times a_v) \right|_{E_{IN}, A_V} = A_V, \quad (3.14)$$

$$\left. \frac{\delta}{\delta a_v} (e_{in} \times a_v) \right|_{E_{IN}, A_V} = E_{IN}. \quad (3.15)$$

Thus, I can write the small-signal model of the VGA multiplier as,

$$e_{out} = E_{IN}a_v + A_Ve_{in}. \quad (3.16)$$

Since  $a_v = i_{GAIN}/I_{REF}$ , from Equations 3.11 or 3.12, it is easy to show that a linear model for the nonlinear controller is given by,

$$\left. \frac{da_v}{di_{ED}} \right|_{I_{ED}} = \frac{-\alpha}{I_{ED}} A_V. \quad (3.17)$$

This expression is not in a useful form because it includes the terms  $I_{ED}$  and  $A_V$  which are internal variables in the loop. Equation 3.17 can be rewritten in terms of external variables by substituting the relation,  $I_{ED} = G_{ED}E_{IN}A_V$ . The simplified

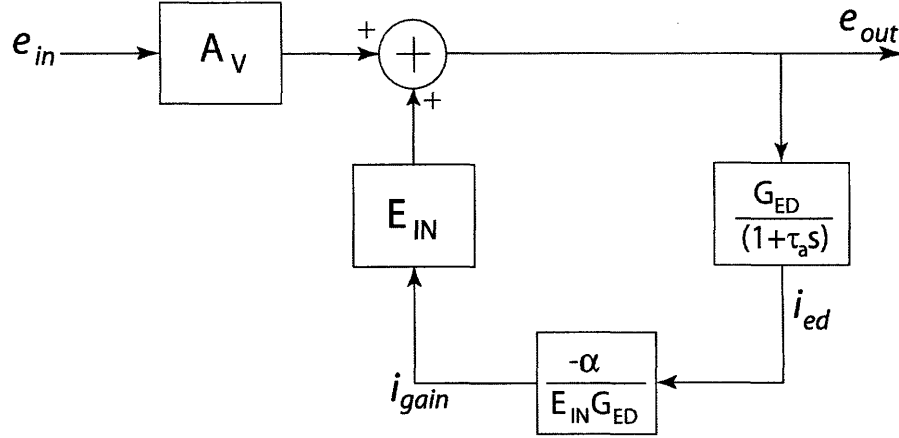


Figure 3-5: Diagram of linearized loop. The loop variables correspond to small-signal envelopes,  $e_{in}$  and  $e_{out}$ , or rectifier or control currents,  $i_{ed}$  and  $i_{gain}$ .

form,

$$\frac{da_V}{di_{ED}} = \frac{-\alpha}{G_{ED}E_{IN}}, \quad (3.18)$$

is much more useful. The overall small-signal linear model is shown in Figure 3-5 in a feedback loop. The loop transmission  $L(s)$  which is negative and independent of  $G_{ED}$  and  $E_{IN}$ , depends on  $\alpha$  and  $\tau_a$ , and is given by,

$$L(s) = \frac{-\alpha}{(1 + \tau_a s)}. \quad (3.19)$$

Intuitively, high values of  $E_{IN}$  or  $G_{ED}$  will turn up the loop transmission since they increase the small-signal gain of the multiplier and envelope detector respectively; however, they also result in a proportionately higher value of  $I_{ED}$  and turn down the small-signal gain of the nonlinear controller like  $1/I_{ED}$  making the overall loop transmission invariant to  $G_{ED}$  or  $E_{IN}$ . Any controller with a power-law nonlinearity and a multiplication nonlinearity in a feedback loop will exhibit such level-invariant loop transmission.

There are two major advantages of a level-invariant loop transmission: First, once the loop dynamics are set by the parameters,  $\tau_a$  and  $\alpha$ , the closed-loop AGC



dynamics are invariant with level and robust to variations in talker distance, talker effort, or microphone sensitivity. Second, additional time constants in the loop may degrade the phase margin of the loop, and cause overshoot, ringing, and other second-order behavior. The level-invariant property ensures that if the loop is stable and has satisfactory tracking dynamics at one level, then it will be stable and have satisfactory tracking dynamics at all levels. I will later demonstrate level-invariant closed-loop AGC responses. For the AGC in this chapter, the closed-loop behavior is nearly first-order. In a brief conference publication, I have demonstrated level-invariant second-order closed-loop behavior as well [35].

Although level-invariant behavior is simple and has its advantages, it is often desirable to adapt more rapidly to louder transients than to softer transients as is observed in the human auditory system during forward masking [42]. I will now discuss a dual-loop AGC that is capable of altering its dynamics depending on the nature of the change in its input and on its past history. This AGC was developed to better meet patient's needs in real hearing environments.

### 3.3 Dual-Loop AGC

My approach to employing a dual set of time-constants follows work in AGCs developed for hearing aids [33][43]. The Moore algorithm uses two sets of attack-and-release time constants to give patients improved listening experience. One slow set, typically in the range of hundreds of milliseconds, operates under normal circumstances. The faster set, typically tens of milliseconds, operates on sudden transients. In addition, the algorithm employs a timer which holds the slow control and prevents it from releasing under certain conditions. My system implements a slightly simplified version of the algorithm which is illustrated in the waveforms of Figure 3-6, diagrammed in the architecture of Figure 3-6, and described below. The algorithm helps with speech processing in noisy environments in two ways: First, the hold timer prevents the gain from changing rapidly during brief silences in speech, and in between vowels, preventing the unnecessary amplification of noise. Second, the faster adaptation helps

the AGC cope with sudden transients in the environment like a door slam. Thus, speech sounds shortly after a loud signal are still intelligible and not attenuated by the recovery of a slow controller.

### 3.3.1 The Dual-loop algorithm

Example waveforms that illustrate the functioning of the Moore algorithm are shown in Figure 3-6. Five waveforms are shown. The topmost is the envelope of the input signal. The response of an envelope detector with fast time constants to this input is shown below it. An envelope detector with slower time constants also responds to the input envelope, but its response is conditioned by a hold timer on falling input envelopes. The slow detector only tracks falling input envelopes if a hold timer has been discharged and holds its state. Otherwise, rising input envelopes do not condition the tracking of the slow envelope detector by the hold timer. The hold timer charges whenever the fast envelope exceeds the slow envelope indicating an increasing transient. It discharges whenever the fast envelope falls below the slow envelope indicating a decreasing transient, or when the fast and slow envelope have become nearly equal. Otherwise, it holds its state. It cannot charge beyond or discharge below a maximum and minimum level respectively. The gain of the AGC is conservatively determined by the larger of the fast or slow envelopes except that the fast envelope is attenuated by 0.4 (8dB attenuation) before this comparison. Thus, the fast envelope can only seize control if it is significantly above the slow envelope. To prevent jitter, the slow envelope is only allowed to regain control once it has lost it, when the fast envelope is one half of the slow envelope (6dB attenuation).

The waveform at the bottom of Figure 3-5 shows the output response of the AGC due to these interactions. Attacks and releases result in positive and negative derivative responses respectively as the AGC adapts its gain to the transient. Holds cause derivative responses that are delayed after the transient and are only seen for falling transients.

Before the presence of any transients in the input envelope, the hold-timer condition has discharged to its lowest level because both the slow and fast envelope filters

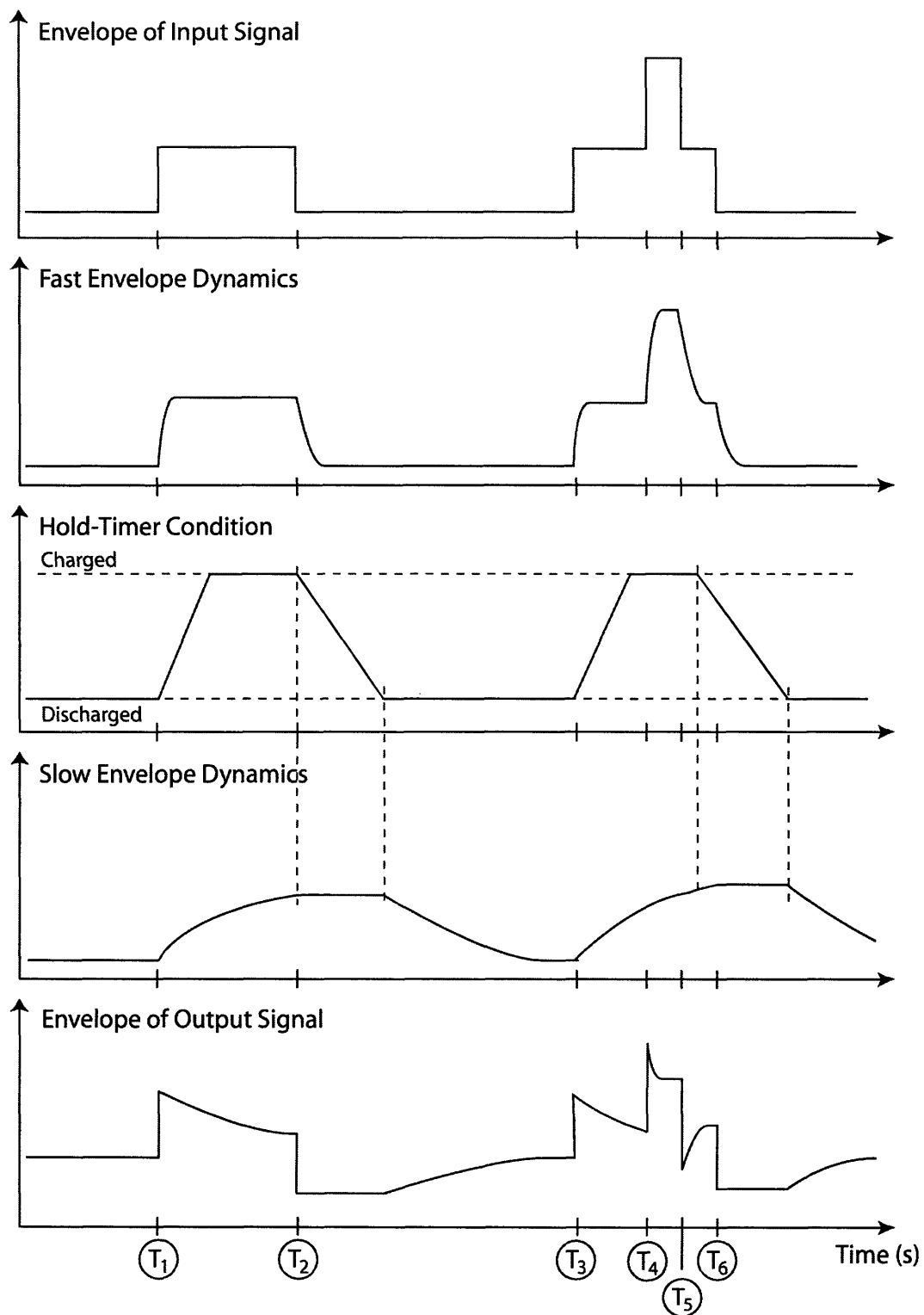


Figure 3-6: An outline of the dual-loop operation on a hypothetical input envelope. Note that the hold-timer condition informs the release of the slow envelope filter.

have equilibrated to a constant and equal level. A transient is applied at time labeled  $T_1$ . Both the fast and slow envelope filters respond to the transient with  $\tau_{a, Fast}$  and  $\tau_{a, Slow}$ , respectively. The hold-timer begins to charge because the fast envelope exceeds the slow envelope indicating an increasing transient. After the charging time,  $T_{charge}$ , the hold-timer becomes fully charged and remains so because the slow envelope remains below the fast envelope for a while.

At time  $T_2$ , the input envelope falls, and the fast envelope falls quickly such that it is now below the slow envelope. The hold-timer senses a decreasing transient and begins to discharge. The slow envelope is not allowed to fall or release until the hold timer has completely discharged at time  $T_2 + T_{discharge}$ .

Another rising transient begins at  $T_3$  and the slow envelope, fast envelope, and hold timer repeat the behavior seen for the transient at  $T_1$ . During this second transient, however, an additional brief loud pulse, e.g., due to a door slam, is superimposed on the second transient from  $T_4$  to  $T_5$ . Since the pulse is much louder than the background level, the fast envelope soon exceeds the slow envelope by more than 8dB (factor of 2.5). The AGC switches to using the fast envelope to determine its gain so that its gain decreases more rapidly. During the short duration of the brief pulse, the slow envelope filter does not respond noticeably. When the pulse ends, the AGC has a fast release as the fast envelope output falls, and when the fast envelope has nearly settled back to its value before the pulse, control returns to the slow envelope.

At  $T_6$ , the input envelope decreases. The slow envelope, however, does not fall until the hold timer is completely discharged. Consequently, the AGC output has a delayed release response.

### 3.3.2 Circuit Implementation of the Dual-loop Algorithm

The architecture of the dual-loop controller is diagrammed in Figure 3-7. The AGC output voltage,  $v_{OUT}$ , drives a rectifier which in turn drives two peak detectors instead of one. One peak detector has fast attack/release properties with a typical attack time constant  $\tau_a = 4ms$  and a typical release time-constant,  $\tau_r = 70ms$ . The slow peak detector has a typical attack time-constant,  $\tau_a = 300ms$  and a typical release

time-constant  $\tau_r = 1000ms$ . Decision circuits, implemented with comparators, the 8dB/6dB attenuator, and current switches, control whether the fast-peak-detector output or slow-peak-detector output is used to drive the translinear controller and the VGA. The hold timer is implemented with simple current sources that charge and discharge the state of its capacitor. The charging time is typically 300ms and the discharging time is typically 600ms. Switches, controlled by simple state logic, charge the hold timer if the fast envelope exceeds the slow envelope, and discharge it if the fast envelope is below the slow envelope. Since the fast envelope always has more ripple than the slow envelope, its average value is always lower than that of the slow envelope when they have both settled. When the fast envelope and slow envelope are nearly equal, the hold timer discharges. This allows an automatic implementation of the condition in the dual-loop algorithm that requires hold timer discharge, that is when the fast and slow envelopes are nearly equal. Comparators output logical signals that indicate that the hold timer is fully charged if its capacitor voltage exceeds a maximum, and that it is fully discharged if its capacitor voltage is below a minimum. The hold-timer state logic then turns off the charging or discharging of the hold-timer capacitor. As long as the hold timer is not fully discharged, a current that determines the dynamics of release in the slow peak detector is switched off.

The current comparator, current switches, charge-pump, 8dB/6dB attenuator and hold-timer state logic blocks of Figure 3-7 are described in Figure 3-8A, 3-8B, 3-8C, 3-8D, and 3-8E respectively. The two current comparators in Figure 3-7 that compare attenuated and unattenuated versions of the fast envelope current with the slow envelope current are implemented as shown in Figure 3-8A with simple cascoded current mirrors, a differential pair, and an inverter. The switches  $M_7$  and  $M_8$  shown in Figure 3-8B allow either  $I_1$  or  $I_2$  to be steered to the output, and therefore, allow either the slow envelope current or fast envelope current to be input to the translinear controller. The hold-timer charge-pump is shown in Figure 3-8C. Simple differential pair, current mirror and cascode circuits are used to generate its logical outputs. The reset switch,  $M_9$ , is included for test purposes.

The 8dB/6dB attenuator is shown in Figure 3-8D: If  $V_{6dB}$  is on, the triode switch

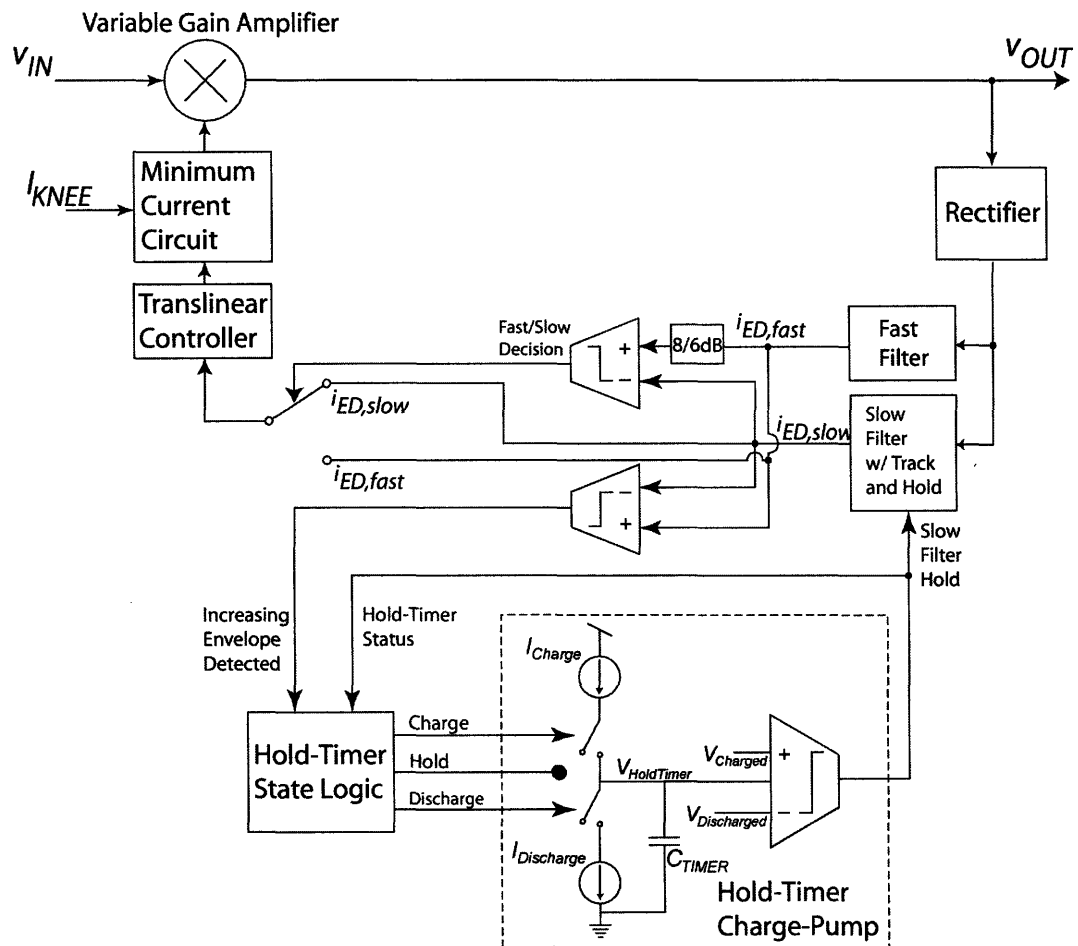


Figure 3-7: Circuit blocks for the dual-loop controller, including the charge-pump structure of the hold-timer.

$M_{21}$  steers current from  $M_{20}$  to the output such that a current-mirror attenuator with a gain of  $(4+1)/10 = 0.5$  is implemented; if  $V_{6dB}$  is off, the current-mirror attenuator has a gain of  $4/10 = 0.4$ . Simple state-logic blocks are shown in Figure 3-8E: This logic ensures that the charging and discharging of the hold timer are only performed if it is not fully charged or fully discharged respectively.

Explicit state storage is not used in these circuits to save valuable chip area. Rather, my system implements implicit asynchronous state-machine control with current-mode computation. My hybrid controller is a simple instantiation of a general class of machines termed hybrid state machines (HSMs) [44].

### 3.4 Experimental Results

Both single- and dual-loop systems were fabricated in  $1.5\mu m$  BiCMOS through the AMI foundry. Both designs performed at low-power as expected. The single-loop controller system was implemented on a  $2.1mm \times 2.1mm$  die with current-mode programming. Operating at 2.8V with a peak current consumption of  $9 - 11\mu A$ , the system demonstrates operation at  $32\mu W$  with 78dB of input dynamic range. Figure 3-9 shows a die-photo of the single-loop AGC chip. The effective loading of the variable-gain amplifier output was 3pF computed from the observed 3dB rolloff at  $9.6kHz$ .

The dual-loop controller chip (shown in Figure 3-10) is  $2.1mm \times 2.1mm$  in size with on-chip 4-bit programming for the compression factor  $\alpha$ , 4-bit programming for the maximum knee current,  $I_{MAX}$ , and 2-bit programming for each of the four fast/slow, attack/release time-constants for a total of 16-bits of programming. On-chip latches store these bits before they are processed by current-mode DACs. The DACs are biased with reference currents obtained from power-supply-noise-immune and temperature-insensitive biasing circuits [36][41].

Figure 3-10 shows a die-photo of the dual-loop controller chip. Operating from 2.8V supply, the peak current consumption of the dual-loop AGC and controller was  $10 - 13\mu A$ , demonstrating  $36\mu W$  performance. The state-machine consumed  $1.4\mu W$ ,

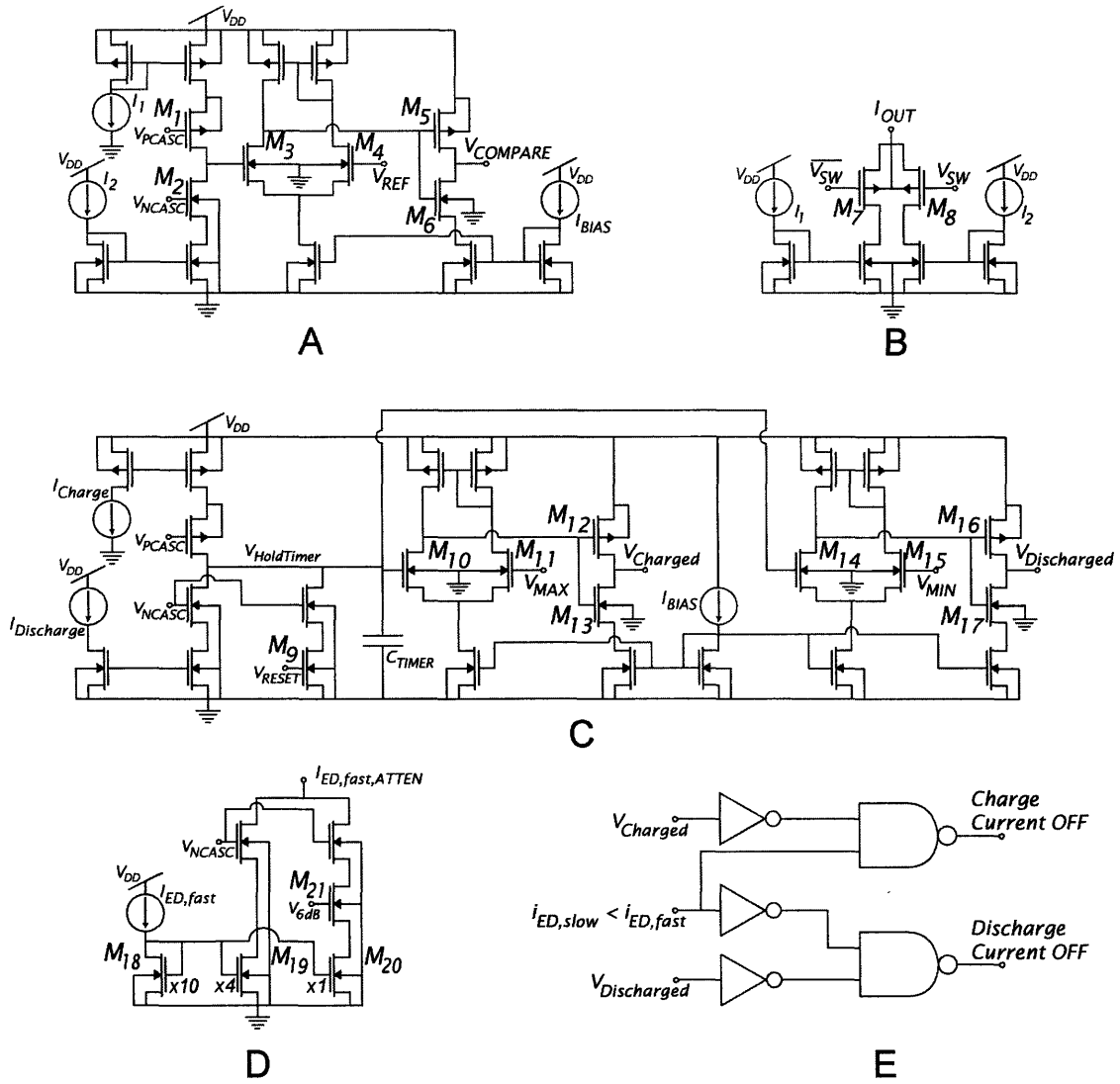


Figure 3-8: Dual-loop controller circuits including the current comparator (A) employing a high impedance current subtractor and a voltage amplifier. The current switching circuit (B) uses two pMOS triode switches to choose between input currents  $I_1$  and  $I_2$ . A charge-pump implements the hold-timer (C). To determine the state of the charge-pump voltage,  $V_{HoldTimer}$ , two open-loop voltage amplifiers are included. The selectable attenuator for the fast filter current is shown in (D). State-logic shown in (E) is included to prevent over-charging or under-charging conditions for the hold-timer. The W/L's of all transistors are  $8\mu m/3.2\mu m$ . The current bias for the inverters,  $I_{BIAS}$ , was chosen to be approximately 30nA.



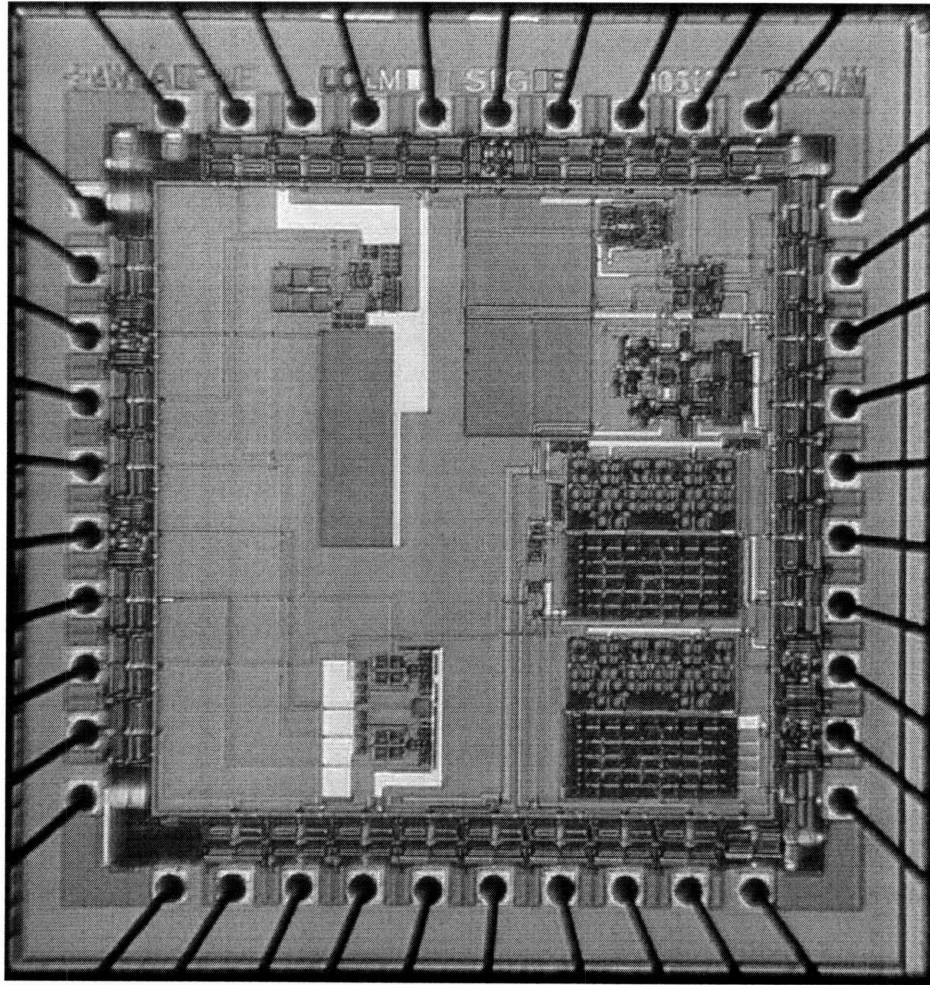


Figure 3-9: Single-loop controller AGC chip.

the hold-timer consumed  $2\mu W$ , and the additional circuitry consumed  $0.6\mu W$ . The total power of the dual-loop AGC is slightly higher than that of the single-loop AGC. Under typical operating conditions; however, the supply current does not exceed  $12\mu A$ . The effective 3dB rolloff was also  $9.6\text{-kHz}$  for this configuration as the VGA was the same in both configurations. The dual-loop AGC was designed to be digitally programmable. The programming ranges, time-constants, and the number of bits for each parameter are shown in Table 3.1. The power consumption of the single-loop AGC system is summarized in Table 3.2. For the dual-loop AGC system the power consumption is summarized in Table 3.3.

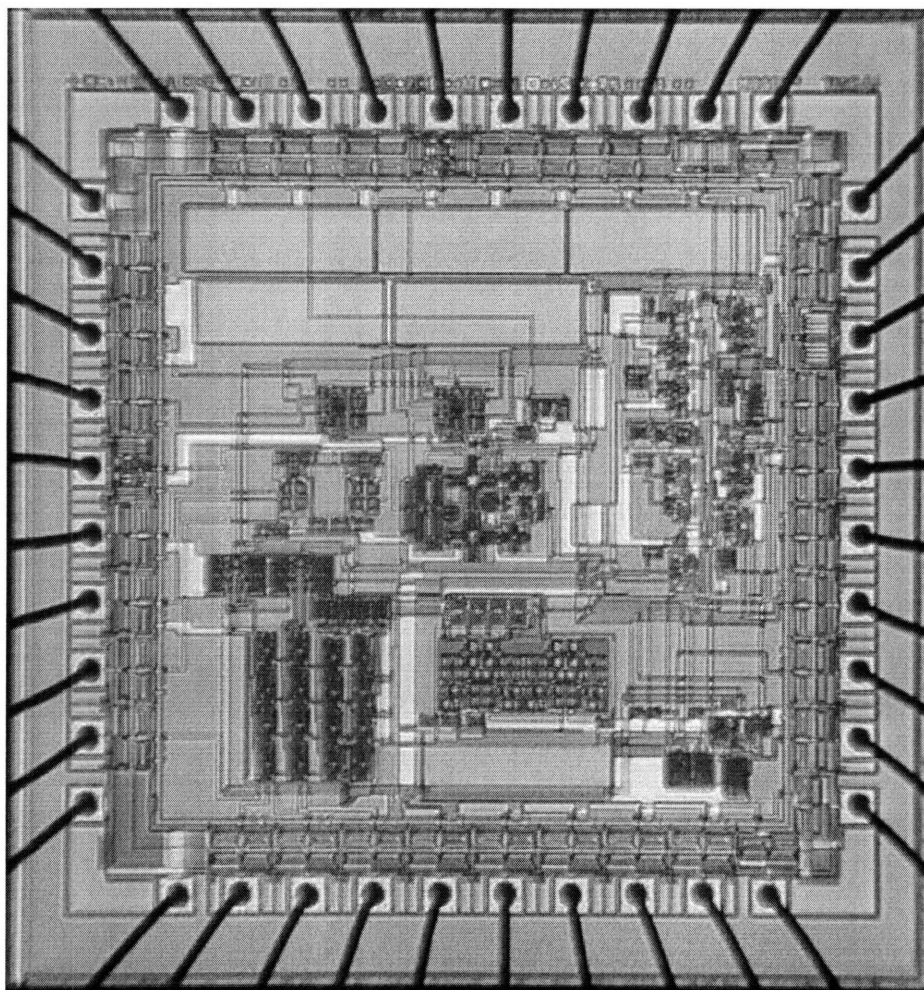


Figure 3-10: Dual-loop controller AGC chip. This die includes a parallel digital programming channel for six separate parameters in the dual-loop design.

Table 3.1: Dual-Loop System Programming Properties

Programming Function	Number of Bits	Programmed Range
$\alpha$ (CR)	4	1 - 1.47
Maximum Gain (Knee point)	4	$0.91 - 11.7 V_{RMS,Out}/V_{RMS,In}$
$\tau_{atk,fast}$	2	1ms - 3ms
$\tau_{atk,slow}$	2	150ms - 300ms
$\tau_{rel,fast}$	2	70ms - 140ms
$\tau_{rel,slow}$	2	900ms - 1800ms

Table 3.2: Single-Loop Controller Power Consumption

Function	Current Consumption @ $V_{DD} = 2.8V$
Variable Gain Amplifier	$400nA - 6\mu A$
Envelope Detector	$910nA$
Peak Detector	$50nA$
Translinear Controller	$200nA - 1\mu A$ Programmed
Biasing Circuits	$1.84\mu A$
Total Power Consumption Range	$< 9.8\mu A$ ( $27\mu W$ )

### 3.4.1 Variable Gain Amplifier

I tested the variable gain subsystem for linearity, noise, and instantaneous output signal-to-noise ratio. The power consumption of the VGA varied between  $230nA - 3\mu A$  as the gain varied from approximately 1 to 13. The maximum output signal amplitude,  $v_{MAX}$ , at 1% Total Harmonic Distortion (THD) was largely invariant with gain level suggesting that distortion is dominated by the output resistance in the VGA rather than by the input V-to-I transductor. The corresponding maximum input signal amplitude is obtained by dividing  $v_{MAX}$  by the gain. It was maximum at a gain of 1, with a measured value of  $405mV_{rms}$ . Figure 3-11 shows that  $v_{MAX}$  does have some dependence on the gain due to nonlinear effects in the V-to-I transconductor. As the gain increases,  $v_{MAX}$  initially increases because more current is available to reduce slewing effects in the V-to-I transconductor, and the input signal amplitude at  $v_{MAX}$  falls with gain. At the largest gains the V-to-I transconductor is forced into moderate inversion operation such that transistor saturation voltages at the output of the transconductor reduce and  $v_{MAX}$  falls.

Output noise for the VGA is shown in Figure 3-12. Theoretical predictions of the

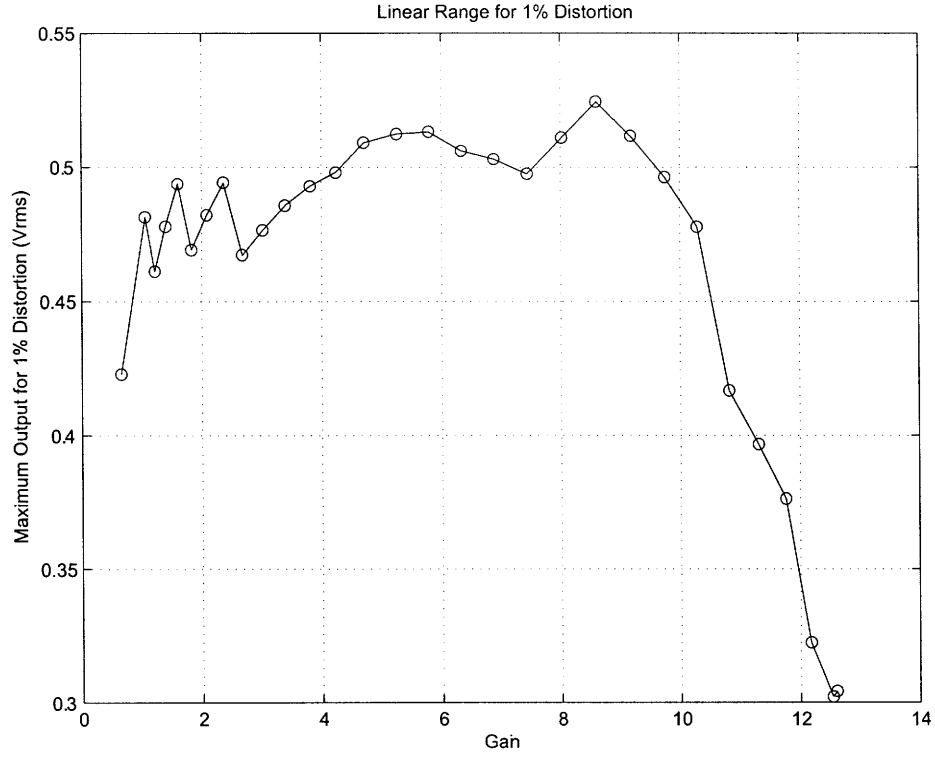


Figure 3-11: Maximum output signal of the variable gain amplifier for 1% THD at varying gain levels. The test frequency was  $1\text{-kHz}$ .

Table 3.3: Dual-Loop Controller Power Consumption

Function	Current Consumption @ $V_{DD} = 2.8V$
Variable Gain Amplifier	$400nA - 6\mu A$
Envelope Detector	$913nA$
Peak Detectors (2)	$103nA$
Dual Controller	$1\mu A$
Translinear Controller	$200nA - 1\mu A$ Programmed
Biasing Circuits	$3\mu A$
Total Power Consumption Range	$< 12\mu A$ ( $34\mu A$ )

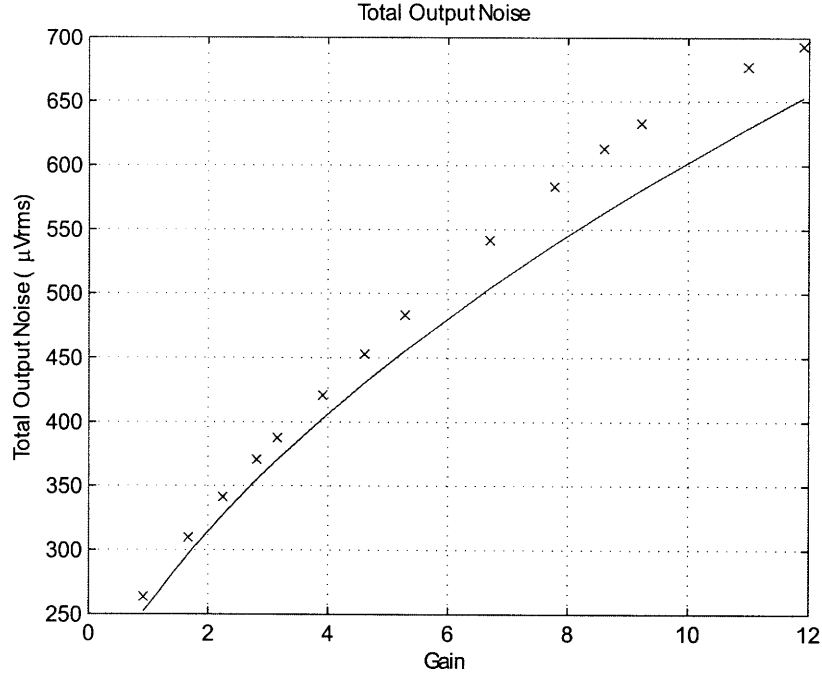


Figure 3-12: Total output noise at the  $v_{OUT}$  node is integrated from 30- $Hz$  to 100- $kHz$ . The solid line represents white noise modeled from Eq. 3.6. Theory and data curves diverge at high gains owing to the relatively larger presence of  $1/f$  noise at these bias currents, which is not modeled in Eq. 3.6.

noise from Equation 3.6 are also plotted. I observe good agreement at lower gains. At higher gains the theory and measured performance begin to diverge somewhat owing to the relatively greater presence of  $1/f$  noise in moderate and strong inversion [38], which I did not model in Equation 3.6. At the highest gain of 11 within my power specification, the output noise is near  $680\mu V_{rms}$  and the input-referred noise is  $62\mu V_{rms}$ .

Two measures of the amplifier dynamic range are relevant for characterizing an AGC. The first is the maximum possible input dynamic range which is defined as the ratio of maximum acceptable input signal at the lowest gain after the AGC has adapted, to the minimum detectable input signal, at the highest gain after the AGC has adapted. This measure determines the overall dynamic range at the input that will be faithfully represented by the AGC. My AGC system dynamic range is 78dB for a 1% THD. The second measure is the instantaneous input dynamic range (IDR) from

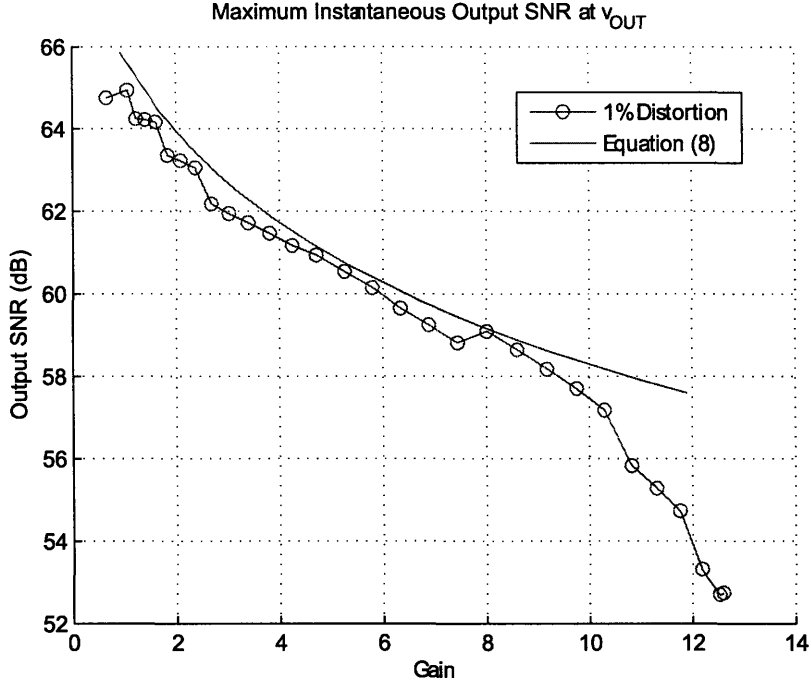


Figure 3-13: Maximum instantaneous output SNR versus gain for a 1 % distortion limit. Note that this is a decreasing function of the gain as more gain increases the output noise. Theory from Eq. 3.8 is shown in the solid line with a constant linear range,  $V_L$ .

the circuit which, at a fixed gain, is also the maximum output signal-to-noise ratio. Figure 3-13 shows the IDR and the theoretical bound on the IDR from Equation 3.8. Except for the largest gains where unmodeled  $1/f$  noise is important, theory and experiment are in good agreement. The AGC's dynamic range is determined by the VGA's dynamic range since I ensured, theoretically, and verified experimentally, that all other controller circuits contributed negligibly to noise and distortion.

### 3.4.2 Single-Loop AGC

I obtained compression and distortion measurements by applying sinusoidal inputs to the single-loop AGC. I also applied speech and audio signals to the system for listening tests using a microphone preamplifier with output dynamic range matched to the input dynamic range of this system [31]. I tested the dynamics of the AGC

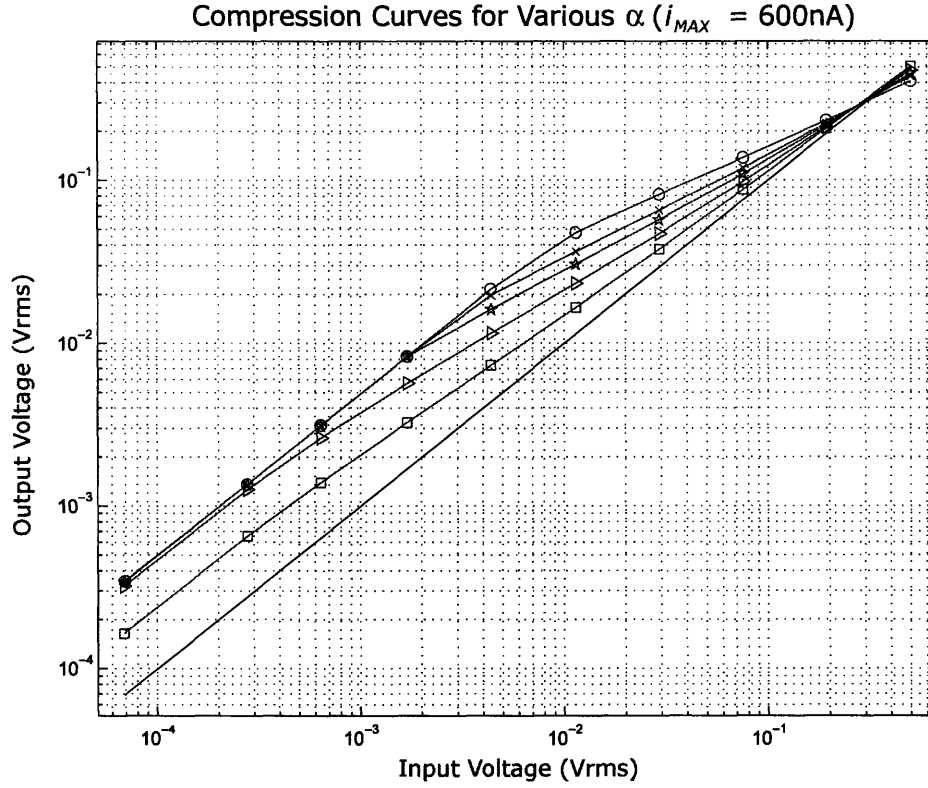


Figure 3-14: Compression curves for varying  $\alpha = \{1.07, 1.16, 1.33, 1.43, 1.67\}$ . A knee was imposed using the max circuit to enforce maximum gain current,  $A_V = 600nA$ . These data were taken from the single-loop AGC.

with tone bursts to represent changing input envelopes.

## Gain

Figure 3-14 shows a set of compression curves for the single-loop system when a maximum gain is enforced using the max circuit. For this example, a maximum gain of 6 was set with  $I_{MAX} = 600nA$ . The compression programming was controlled by a 4-bit DAC. Peak gain error owing to mismatch in the translinear circuit was limited to 8% over the ten tested circuits.

## Dynamic Performance

The closed-loop transfer function for small-signal inputs obtained from Figure 3-5 and Black's feedback formula is given by

$$\frac{e_{OUT}}{e_{IN}} = \left( \frac{A_V}{\alpha + 1} \right) \frac{1 + \tau_a s}{1 + \frac{\tau_a}{\alpha + 1} s}. \quad (3.20)$$

Step response dynamics are governed by the pole at,  $\omega = (\alpha + 1)/\tau_a = CR/\tau_a$ . Note that,  $\alpha + 1 = CR$ , such that as the compression ratio increases, the closed-loop response to transients becomes faster. I determined the consistency of this analysis from step-response measurements. Figure 3-15 shows the measured closed-loop response versus the compression ratio. As predicted, the time constant is reduced with the compression ratio. At higher compression ratios, there is more deviation from theory due to increased effects of other parasitic time constants in the loop. The experimental data of Figure 3-16 shows that the closed-loop time constant of the AGC changes by only 15% over a 60dB change in input intensity demonstrating relatively level invariant behavior. Over this range, the feedback gain-control current changes by a factor of 4.5 in the  $CR = 1.3$  case, and by a factor of 14 in the  $CR = 1.66$  case.

### 3.4.3 Dual-Loop AGC

Since the dual-loop AGC has the same VGA circuit as the single-loop AGC, its noise properties are virtually identical to that of the single-loop AGC. Similarly, its long-term compression and knee characteristics are identical for the same settings. Its primary difference from the single-loop AGC lies in its more complex adaptation dynamics. Therefore, I will only focus on these dynamics.

Two simple control experiments demonstrated that the dual-loop AGC was working correctly. First, the application of sudden transients triggered the action of the fast loop speeding up AGC dynamics. Second, during normal listening, i.e., in the absence of fast transients, the hold-timer charged during increasing sound envelopes,



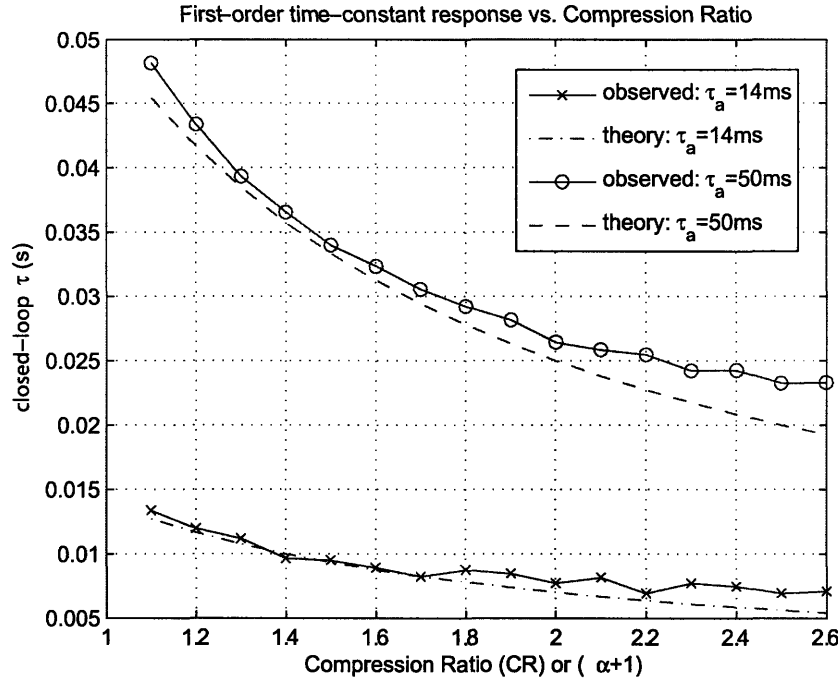


Figure 3-15: Closed-loop time constants for the single-loop controller.

and discharged during decreasing sound envelopes.

Figure 3-17 shows the operation of the dual-loop AGC system under conditions similar to those diagrammed in Figure 3-6. The AGC was configured with  $T_{charge}$  of 300ms and  $T_{discharge}$  of 450ms for the hold timer. The input had two sets of 1-kHz tone-bursts. The first tone-burst had a 50% modulation ratio and lasted from 500ms to 1s. The second tone-burst began at 2.5s with a 50% modulation ratio and changed to 85% modulation ratio for a brief 100ms pulse at 2.75ms. The voltage output response,  $v_{OUT}$ , shows slow adaptation to the smaller tone-bursts with an attack time-constant of  $\tau_{a,slow} = 300\text{ms}$ . During each of the smaller tone-bursts, the hold-timer is active, charging while the slow loop continues to adapt to the sound level. At the end of each tone-burst, the sound level is reduced and the hold-timer discharges. The system successfully holds the slow-loop filter release condition to prevent rapid gain adaptation. Only when the hold-timer has discharged does the gain current, shown below the hold-timer voltage, begin to increase again with a slow-loop release time-constant of  $\tau_{r,slow} = 1.5\text{s}$ .

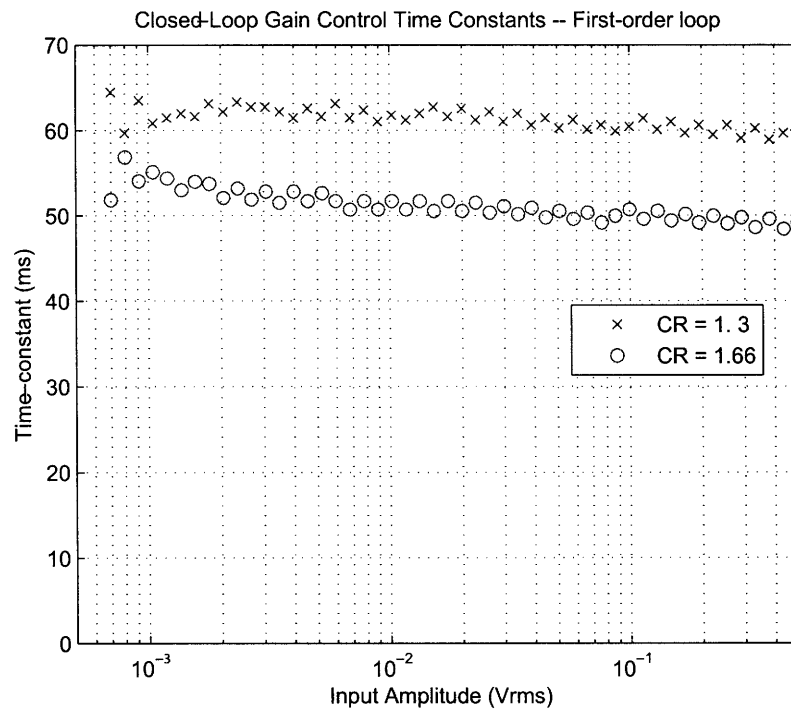


Figure 3-16: Closed-loop time constants for the single-loop controller versus input level. The open-loop attack time constant  $\tau_a$  was set to 80ms.

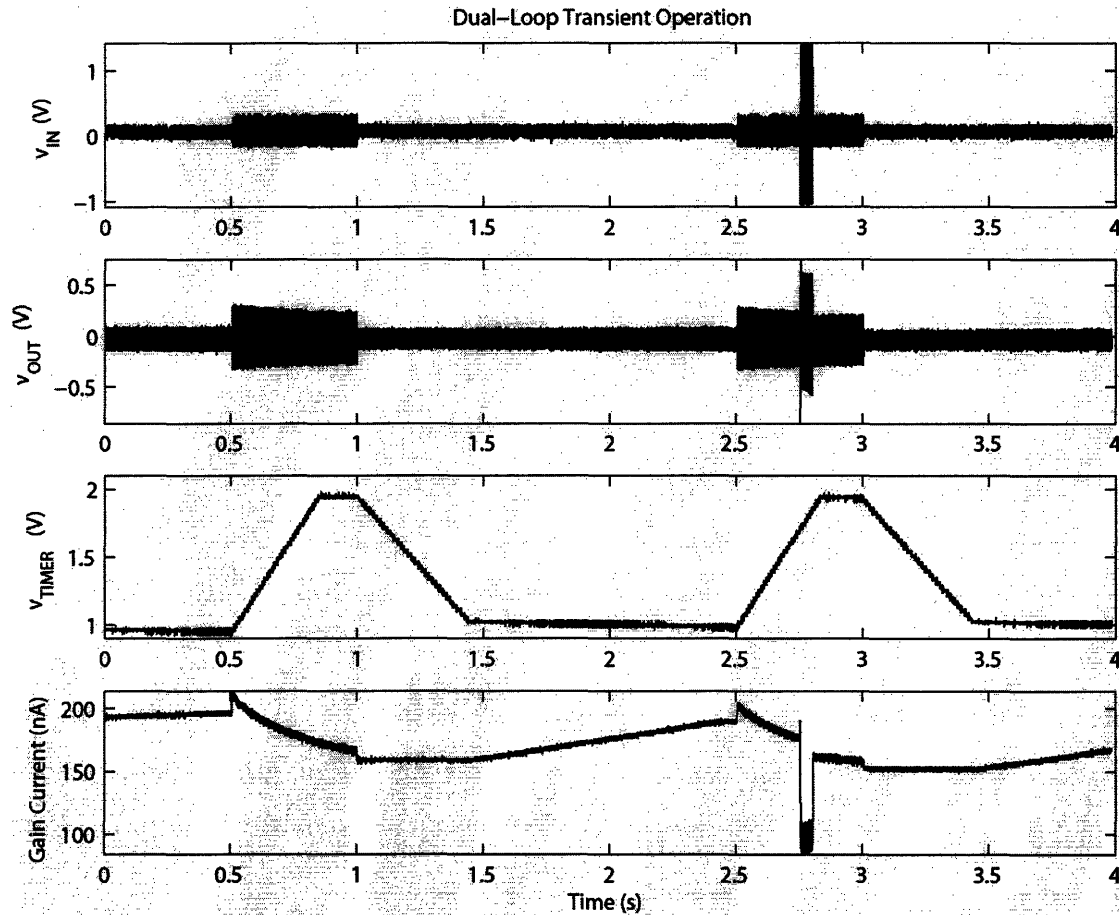


Figure 3-17: A transient response of the dual-loop controller. The input waveform  $v_{IN}$  is designed to excite several of the relevant conditions for the hybrid controller. The background sound is a 1-kHz sinusoid with tone-bursts presented at 0.5s and 2.5s. At 2.75s, a larger tone is presented with 100ms duration, intended to represent a loud transient and trigger the fast response loop. The output voltage  $v_{OUT}$  is shown below the input voltage trace and indicates slow-loop adaptation in gain for each tone-burst. The gain release does not begin until the hold-timer has discharged to its resting level. This can be seen in the gain current shown at the bottom. When the loud transient occurs, at 2.75s, the gain is reduced rapidly, corresponding to the fast-loop attack time constant.

The loud transient at 2.75s in Figure 3-17 excites the fast-loop. The gain decreases so rapidly, i.e. with  $\tau_{a, Fast} = 4ms$ , that relative to the figure scale the event appears as a vertical line in the output voltage plot. Because the slow-loop filter output never catches up with the fast-loop filter output, the hold-timer continues to charge during this period. When the loud transient subsides, the system returns to normal slow-loop operation.

### 3.5 Summary

In this chapter, I have presented single-loop and dual-loop AGCs for bionic ears with a dynamic range of 78dB, a power consumption less than  $36\mu W$ , and an instantaneous dynamic range of operation of 58dB for typical settings.

As predicted by the mathematics of log-linear feedback loops, experimental observations of closed-loop dynamics are level invariant and speed up as the compression ratio of the AGC is increased. Theoretical analyses of noise, dynamic range, and power are in good accord with measured experimental results.

Gain control systems are a crucial part of any low-power wide-dynamic-range signal processing system. By using gain control to manage signal-to-noise ratio, I can reduce the overall power consumption of my internal bionic-ear circuitry because it operates with relaxed noise and linearity constraints without losing any important information about the signal. I will briefly discuss a bionic ear processor which meets these needs in Chapter 5 where a bionic ear system with suitable internal dynamic range is described.

Patient listening comfort in noisy environments is also influenced by the type of compression algorithm used. To improve patient comfort, my dual-loop AGC was capable of being digitally programmed, exhibited closed-loop dynamics consistent with the Moore algorithm for hearing aids, and was implemented as a novel hybrid state-machine-and-analog-control feedback circuit. This hybrid analog-digital control approach allows me to implement an algorithm, with asynchronous state decisions, to be implemented without a full A/D-DSP system [5].

These AGCs are useful in both analog and digital bionic ear processors, as a front end prior to analog spectral analysis or before A/D conversion. If they are used in conjunction with a charge pump, to enable low voltage operation, they may also be used as front ends in low-power hearing-aid processors.



## Chapter 4

# Feedback Analysis and Design of RF Power Links for Low-Power Bionic Systems

Implanted electronics are used in medical devices for diagnosis as well as for treatment of a wide variety of conditions – pacemakers for cardiac arrhythmia, retinal implants for the blind, cochlear implants for deafness, deep-brain stimulators for Parkinson’s disease, spinal-cord stimulators for control of pain, and brain-machine interfaces for paralysis prosthetics. Such devices need to be small and operate with low power to make chronic and portable medical implants possible. They are most often powered by inductive RF links to avoid the need for implanted batteries, which can potentially lose all their charge or necessitate re-surgery if they need to be replaced. Even when such devices have implanted batteries, an increasing trend in upcoming fully implanted systems, wireless recharging of the battery through RF links is periodically necessary<sup>1</sup>.

Figure 4-1 shows the basic structure of an inductive power link system for an example implant. An RF power amplifier drives a primary RF coil which sends power inductively across the skin of the patient to a secondary RF coil. The RF signal on

---

<sup>1</sup>© 2007 IEEE. Reprinted, with permission, from Transactions on Biomedical Circuits and Systems.

the secondary coil is rectified and used to create a power supply that powers internal signal-processing circuits, electrodes and electrode-control circuits, signal-sensing circuits, or telemetry circuits depending on the application. The power consumption of the implanted circuitry is eventually borne by external batteries that power the primary RF coil; if an RF link is energy efficient, most of the energy in the primary RF coil will be transported across the skin and dissipated in circuits in the secondary. It is also important for an RF link to be designed such that the power-supply voltage created in the secondary is relatively invariant to varying link distances between the primary and secondary, due to patient skin-flap-thickness variability, device-placement, and device variability.

Recent advances in signal processing and electrode design have reduced power dissipation in internal circuits considerably. For example, a cochlear implant processor with only  $250\mu W$  of signal-processing power [41][36] can be combined with electrodes that dissipate  $750\mu W$  of power via lowered impedance strategies or low-power stimulation strategies [60] to create cochlear-implant systems that dissipate  $1mW$  of power. Pacemaker systems often run on power levels that range from  $10\mu W$  to  $1mW$  depending on their complexity. RF power links for such systems need to achieve good energy efficiency such that needless amounts of external power are not used to power an efficient internal system. This chapter explores the design of such RF links and builds on prior work in relatively high-power systems. Small losses that are important in low-power systems, may be insignificant in higher-power systems. For example, the retinal-implant design described in [12] is geared towards systems that dissipate near  $250mW$ ; it dissipates  $40mW$  in its closed-loop Class-E power amplifiers alone, which is prohibitive for my intended applications but acceptable in the retinal-implant design. As another example, the design described in [61] is geared towards a link system that is capable of driving amperes of current into the primary portion of the link such that a reasonable amount of power may be received in several tiny secondaries.

A theoretical model of RF links has been described in [62] who focused on operating at conditions of critical coupling. In critically-coupled conditions, the magnitude



of the voltage transfer function from the primary to the secondary is maximized and the voltage is relatively invariant to varying link distances. However, the energy-transfer efficiency has a theoretical maximum of 50% at critical coupling, and actual experimental measurements were found to be in 5% to 32% range, lower than is desirable for my applications. In my work, I have focus on designing for maximum link energy efficiency and obtaining acceptable robustness to inter-coil separation. In this chapter, I derive an explicit loading condition for optimal energy efficiency and show that my measurements are in good accord with theory. My feedback method yields a simple-and-pleasing result that shows that at critical coupling, the feedback-loop transmission is -1, a result in accord with formulas in [62].

The work in [63] describes a clever technique for adapting the operating frequency of a Class-E power amplifier such that good energy efficiency is always maintained independent of the geometry-dependent coupling between the primary and secondary. The technique appears to be more suited to relatively high coupling, requires a tapped primary, and measurements did not include efficiency losses due to rectifier circuits. I have chosen a simpler and different power-amplifier topology in this work to minimize power losses that may be caused by added complexity and to minimize robustness and instability issues caused by more complex Class-E topologies.

I will only focus on issues regarding power transfer since efficient power transfer is the bottleneck in RF links, not efficient data transfer. Several papers have described schemes for sending power and data through the same link [61, 22, 64]. It is worth pointing out that power transfer is more efficient with high-Q coils, a requirement that can conflict with data transfer if a high-bandwidth data link is necessary. Thus, it is often advantageous to optimize power and data transfer at different operating frequencies.

The contributions of this chapter are two-fold: First, I describe a feedback analysis which aides in understanding optimal voltage-transfer and power-transfer functions for coupled resonators from a viewpoint that appears to be simpler than prior algebraic analyses and leads to a methodology for systematic design. Second, I describe the design of a low-power integrated Class-E power amplifier switch and controller

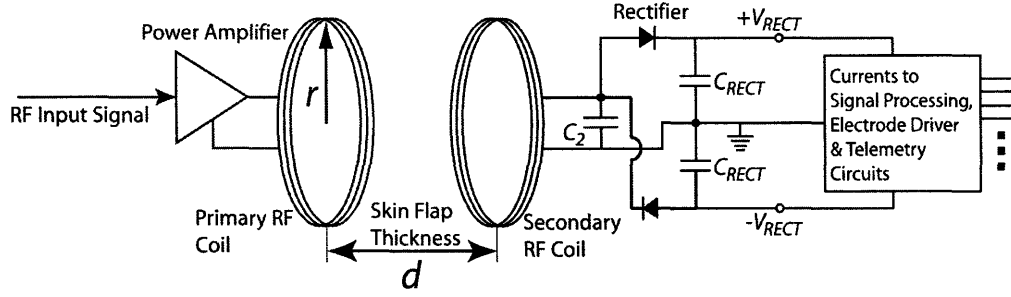


Figure 4-1: An example of a low-power bionic implant system is shown.

that demonstrates sufficiently small loss for a load power of 1mW such that high overall energy efficiency in an RF link is achieved. My overall efficiency measurements also include losses due to rectifier circuits.

This chapter is organized as follows. In Section 4.1, I discuss the theory of linear coupled resonators, the role of feedback, and derive expressions for efficiency. In Section 4.2, I discuss the design of a bionic implant power system, with attention to efficiency at low power levels. In section 4.3, I present experimental results. In Section 4.4, I conclude by summarizing the main contributions of this chapter.

## 4.1 Basic Model of Coupled Resonators in an RF Link

A pair of magnetically coupled resonators are shown in Figure 4-2 and represent a model of the RF link with the primary resonator on the left and the secondary resonator on the right. The mutual inductance between the primary and secondary is represented by  $M$ . The resistances  $R_1$  and  $R_2$  are implicit resistances due to coil losses in the inductances  $L_1$  and  $L_2$  while  $C_1$  and  $C_2$  are explicit capacitances used to create a resonance in the primary and secondary respectively. Using a resonant secondary circuit amplifies the induced voltage and is helpful in overcoming the turn-on voltage of rectifier diodes. A series-resonant primary network requires lower voltage swings at its input because the phase of the inductor and capacitor voltage cancel at resonance.

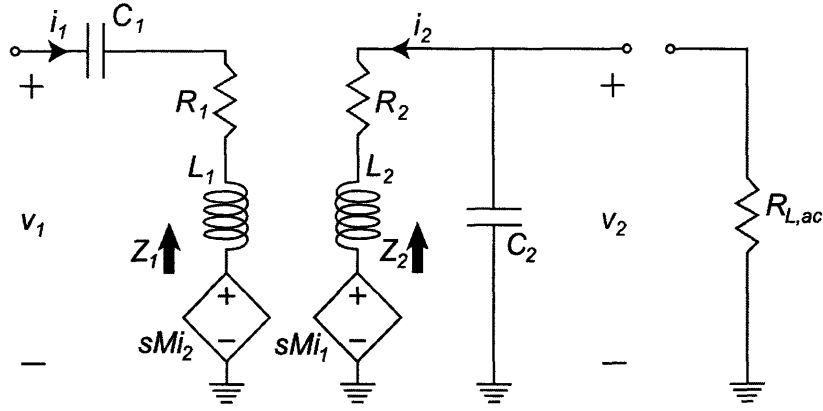


Figure 4-2: Inductively coupled series-parallel resonators. Coupling between the inductors is modelled with dependent voltage sources  $sMi_1$  and  $sMi_2$ .

The rectifier circuit that is in parallel with  $C_2$  has been replaced by an equivalent linear resistance  $R_{L,ac}$  that represents its effect at the RF frequency: If the ripple on the output of the rectifier circuit is small, achieved due to a large load capacitance  $C_{RECT}$  at its output as shown in Figure 4-1, then, since the rectifier output DC voltage is approximately the peak a.c. RF voltage at  $C_2$ , the a.c. r.m.s. energy at RF must be equal to the DC energy dissipated at the resistor by energy conservation; thus,  $R_{L,ac} = R_L/2$ , where  $R_L$  is the effective load of all the internal implanted circuits powered by the rectifier supply created at  $C_{RECT}$ .

The geometric coupling factor between two coils of wire,  $k$ , is the ratio of common flux linkage between the coils. If two coils of wire are placed near each other, the common flux between the two coils cannot exceed the total flux produced by either of the coils. Therefore, for a uniform dielectric environment the coupling factor  $|k| < 1$ . Writing the mutual inductance as the geometric product of the discrete inductances  $M = k\sqrt{L_1 L_2}$ , we can also understand the coupling factor  $k$  as the fraction of induced voltage on one coil due to current in the other coil. We model this dependency with the controlled sources  $sMi_1$ , and  $sMi_2$  in the coupled resonators.

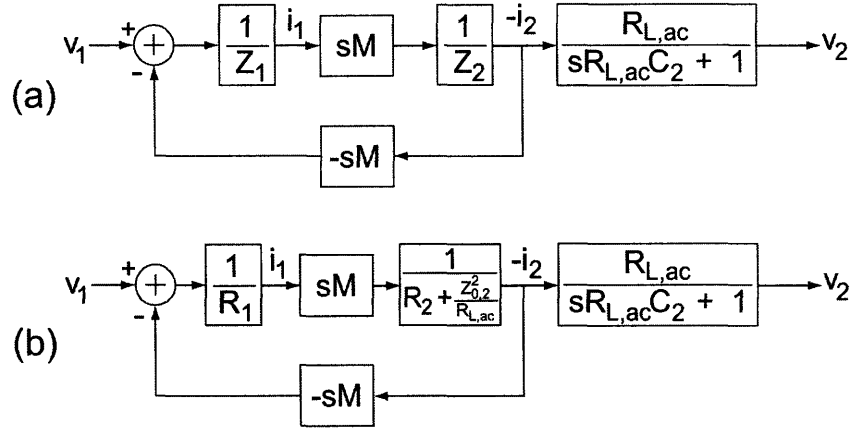


Figure 4-3: Feedback diagrams for coupled resonators in Figure 4-2. The top diagram (a) shows the loop diagram under all frequencies. The bottom diagram (b) shows an approximate loop diagram under resonant conditions  $\omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$ .

#### 4.1.1 Feedback Analysis

The block diagram in Figure 4-3a models the circuit of Figure 4-2. The loop transmission,

$$L(s) = \frac{s^2 M^2}{Z_1(s) Z_2(s)}, \quad (4.1)$$

$$L(j\omega) = \frac{-\omega^2 k^2 L_1 L_2}{Z_1(j\omega) Z_2(j\omega)}, \quad (4.2)$$

is of a form that appears to indicate positive feedback at d.c: The loop transmission  $L(j\omega)$  near  $\omega = 0$  is  $k^2 \omega^4 L_1 C_1 L_2 C_2$  implying a positive loop transmission at and near DC. While this may seem puzzling at first, the loop transmission is easily interpreted as the product of two Lenz's law expressions, each of which implements negative feedback from one coil to another, but whose product is positive. The magnitude of the loop transmission at  $\omega = 0$  is 0 and at  $\omega = \infty$  is  $k^2$ , which is less than 1. The phase and magnitude of the feedback changes with frequency in between these limits according to the expressions above.

The feedback effects can be viewed as creating an effective impedance in the primary circuit due to reflected impedance from the secondary if I evaluate  $sM i_2 / i_1$ .

Using the feedback diagram,

$$\frac{sMi_2}{i_1} = -\frac{s^2M^2}{Z_2} = -Z_1L(s). \quad (4.3)$$

Looking into the input of the primary resonator, the net input impedance  $Z_{in}$  is then given by

$$Z_{in}(s) = Z_1(s) (1 - L(s)). \quad (4.4)$$

As the coupling increases the loop transmission, the input impedance is dominated, first by the primary impedance,  $Z_1(s)$ , and then by the impedance seen in the primary due to reflected secondary loading  $-Z_1(s)L(s)$ . The feedback block diagram in Figure 4-3b shows a simplification of the block diagram under resonant conditions when  $\omega_n \approx \frac{1}{\sqrt{L_1C_1}} \approx \frac{1}{\sqrt{L_2C_2}}$  where  $\frac{Z_{0,2}^2}{R_{L,ac}} = \frac{L_2}{R_{L,ac}C_2}$  is the parallel-to-series impedance transformation of  $R_{L,ac}$  due to the resonator formed by  $L_2$  and  $C_2$ .

### 4.1.2 Root Locus Analysis

A helpful simplification to the loop transmission in the feedback loop in Figure 4-3a is to write the resonators as second-order systems with quality factor  $Q$  and natural frequency  $\omega_n$ ,

$$Z = \frac{s^2 + \frac{sR'}{L} + \frac{1}{LC}}{\frac{s}{L}} = \frac{s^2 + s\frac{\omega_n}{Q} + \omega_n^2}{\frac{s}{L}}. \quad (4.5)$$

where  $R'$  is the effective resistance due to all losses in the primary or secondary. Finding the simplified loop transmission using the bandpass definitions in Equation 4.5,

$$\begin{aligned} L(s) &= \frac{s^2M^2}{Z_1Z_2} = \frac{s^2k^2L_1L_2}{Z_1Z_2} \\ &\simeq \frac{k^2 \frac{s^2}{\omega_{n,1}^2} \frac{s^2}{\omega_{n,2}^2}}{\left( \frac{s^2}{\omega_{n,1}^2} + \frac{s}{\omega_{n,1}Q_1} + 1 \right) \left( \frac{s^2}{\omega_{n,2}^2} + \frac{s}{\omega_{n,2}Q_2} + 1 \right)}. \end{aligned} \quad (4.6)$$

Here, the natural frequencies of the resonators are  $\omega_{n,1}$  and  $\omega_{n,2}$ , respectively.

Under feedback, the open-loop poles associated with each of the resonators move

on the complex plane as the geometric coupling factor  $k$  varies with inter-coil separation or misalignment and changes the root-locus gain. In a retinal implant the eye moves during normal patient activity changing  $k$ . Each of the resonators in Figure 4-2 is characterized by a natural frequency,  $\omega_n$ , and damping factor,  $\zeta = \frac{1}{2Q} = \frac{R}{2\omega L}$ . Ideally the quality factor of each resonator is set by only the effective coil resistances,  $R_1$  and  $R_2$ , and  $R_{L,ac}$ ; however, in a real system, the resistance of the power amplifier, resistance in the capacitors and objects in the environment can all contribute to reducing the effective quality factor of the coils.

Figure 4-4 shows how the four open-loop complex poles move under positive feedback as the root-locus gain parameter  $k^2$  is changed. The techniques used to create this plot are the standard techniques of root locus from feedback theory [30]. The open-loop poles in Figure 4-4(a) are identical and model the case where no loading is applied to the secondary circuit. Now, adding the resistor  $R_{L,ac}$  to model rectifier loading, the damping of the secondary resonators will be different from that of the primary. The open-loop secondary poles appear more damped on the  $\omega_n$  circle, shown in Figure 4-4(b). In this new configuration the poles move along the  $\omega_n$  circle towards one another and then split along the trajectory loci for the unloaded case. The four asymptotes of the root-locus trajectories enter the origin along the positive and negative X-axis and positive and negative Y-axis asymptotes at infinite root-locus gain. It is interesting to note that the root-locus trajectories predict that the lower-frequency closed-loop pole pair that is radially closer to the origin and moving towards it will have a higher quality factor due to their extreme angle of entry, while the closed-loop pole pair that is radially further from the origin and moving away from it will have a lower quality factor due to their less extreme angle of entry. My experimental measurements, presented in Figure 4-7(a) in a future portion of the chapter, confirm this theoretical prediction, a fact that is seen in all prior data in the literature, but that appears to have never been commented on or explained.

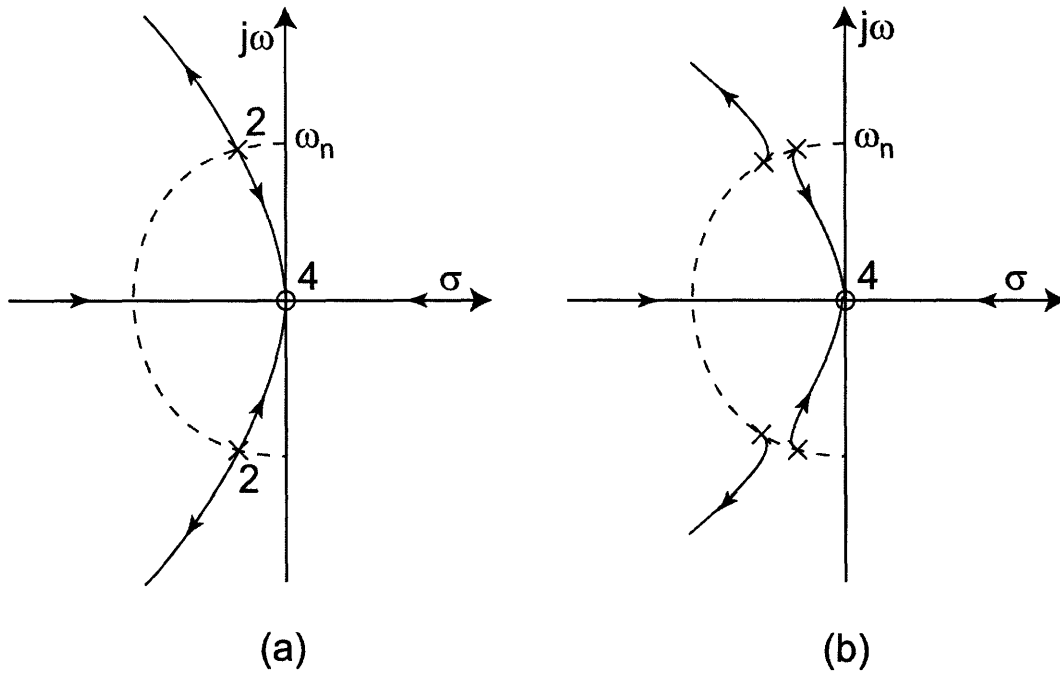


Figure 4-4: Root locus diagrams are shown for two resonator cases. In (a), the resonators are identical. A loaded resonator case (b) will have a higher damping factor due to energy lost to the rectifier. In this case the poles move together before splitting from the constant- $\omega_n$  circle.

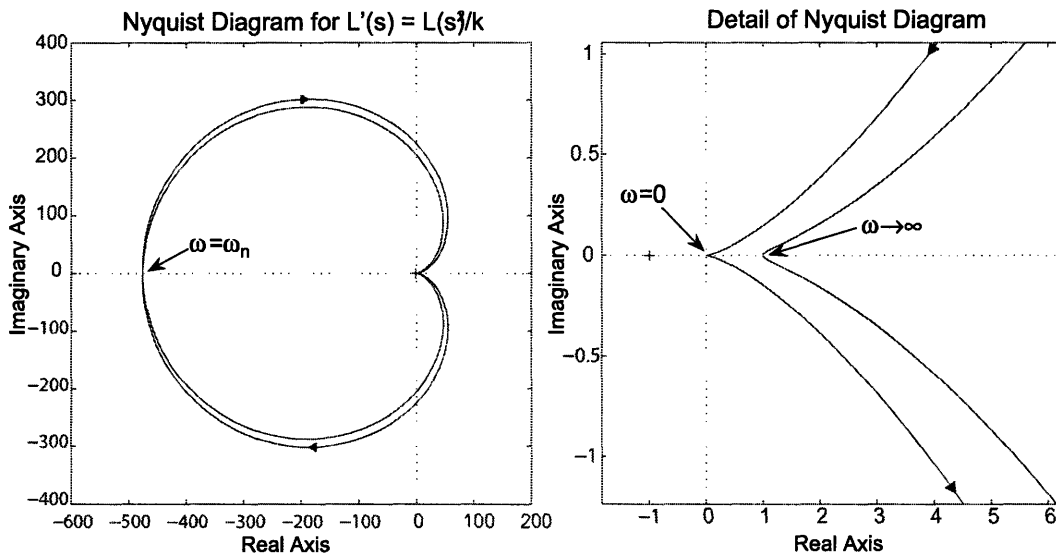


Figure 4-5: An overall Nyquist diagram of  $L(s)/k^2$  is shown in (a) and detail near the origin is shown in (b). As the frequency approaches  $\omega_n$  the Nyquist plot approaches the  $180^\circ$  point with magnitude  $Q_1 Q'_2$ . For  $L(s) = -1$ , and this phase condition we must have  $k = k_c$ .

### 4.1.3 Coupled Resonator Voltage Transfer Function

From the block diagram in Figure 4-3, I can write the transfer function,

$$\begin{aligned}\frac{v_2(s)}{v_1(s)} &= \left( \frac{L(s)}{1 - L(s)} \right) \left( \frac{1}{sM} \right) \left( \frac{R_L}{sC_2R_L + 1} \right) \\ &= \left( \frac{L(s)}{1 - L(s)} \right) \left( \frac{1}{sk\sqrt{L_1L_2}} \right) \left( \frac{R_L}{sC_2R_L + 1} \right) \\ &= \left( \frac{kL'(s)}{1 - k^2L'(s)} \right) \left( \frac{1}{s\sqrt{L_1L_2}} \right) \left( \frac{R_L}{sC_2R_L + 1} \right),\end{aligned}\quad (4.7)$$

where we've defined  $L(s) = k^2L'(s)$  to explicitly indicate the dependence of the loop transmission on the parameter  $k$ . By differentiating the latter equation w.r.t.  $k$  and equating it to zero, it's easy to show that the voltage transfer function has an extremum when  $k^2L'(s) = -1$ , i.e., when the loop transmission  $L(s)$  is -1. Physically, this extremum can be shown to be a maximum: When  $k$  is small, the voltage transfer function is small because there is little coupling of the current in the primary to the dependent voltage source in the secondary; when  $k$  is large, the input impedance seen in the primary  $Z_{in}(s) = Z_1(s)(1 - L(s))$  increases as  $L(s) = k^2L'(s)$  increases with  $k$  such that the current in the primary reduces, decreasing the voltage transfer function. The optimal or critical coupling occurs when  $k^2L'(s) = L(s) = -1$ , at which point the voltage transfer function is maximized. At this value of  $k = k_c$ , the link is said to be critically coupled. Note that at this value  $Z_{in}(s) = 2Z_1(s)$  or equivalently, the reflected impedance of the secondary in the primary,  $-Z_1(s)L(s)$ , is equal to  $Z_1(s)$ .

At resonance, the loop transmission can be further simplified by including the effect of the load resistance,  $R_{L,ac}$ , transformed by the secondary circuit,

$$L(s)|_{\omega_n} = -k^2 \left( \frac{\omega L_1}{R_1} \right) \left( \frac{\omega L_2}{R_2 + \frac{Z_{0,2}^2}{R_{L,ac}}} \right) = -k^2 Q_1 Q'_2. \quad (4.8)$$

where  $Q'_2$  is the loaded  $Q$  of the secondary and implicitly defined as shown. Thus, at critical coupling,

$$k = k_c = \frac{1}{\sqrt{Q_1 Q'_2}}. \quad (4.9)$$



At this critical coupling, since the reflected resistive impedance of the secondary in the primary is equal to the resistive impedance in the primary, 50% of the power of the primary driver is dissipated in the secondary. Thus, the maximum energy efficiency at critical coupling is 50%. The actual energy efficiency is lower than 50% because all of the energy dissipated in the secondary is not dissipated in the load,  $R_{L,ac}$ , but some of it is dissipated in the coil resistance  $R_2$  as well.

The Nyquist plot of  $L'(s) = L(s)/k^2$  is shown in Figure 4-5 such that  $1/k^2$  may be viewed as a gain parameter of the plot. Since  $k^2$  is always less than 1, the  $1/k^2$  point always lies outside the contour that intersects the '1' point, therefore, in this positive-feedback version of the classic Nyquist plot, stability is guaranteed. Note, that at the  $180^\circ$  phase point, each resonator contributes approximately 90 degrees of phase at its natural frequency  $\omega_{n,1} \approx \omega_{n,2} \approx \omega_n$ . The critical coupling point, being a maximum, yields robustness in the primary-secondary voltage gain to variations in inter-coil distance or misalignment, which affect  $k$ .

#### 4.1.4 Limits to Energy Efficiency

As energy flows from the source,  $v_1$ , to the load element  $R_{L,ac}$ , it is diverted or dissipated in two mechanisms. First, energy must couple from the primary circuit to the secondary circuit and this coupling depends on the reflected load of the secondary in the primary. Second, energy in the secondary circuit dissipates either in the load element,  $R_{L,ac}$ , or in the lossy resonator element,  $R_2$ . The secondary circuit is most efficient when operated at resonance,  $\omega_{n,2} = \frac{1}{\sqrt{L_2 C_2}}$ . Choosing the primary circuit with the same series resonance increases the voltage gain between the primary and secondary and minimizes the input voltage at the primary.

#### Primary-Secondary Energy Transfer

Energy delivered to the primary circuit is either dissipated in the intrinsic resistance,  $R_1$ , or delivered to the secondary. Of course, this statement ignores any loss mechanisms which may be present in the surrounding medium. Driving the dependent

source impedance represents the work required to deliver power to the secondary circuit. Thus, the fraction of power transferred to the secondary circuit is the split between power in the intrinsic resistance,  $R_1$ , or the dependent source,  $sMi_2$ . From our feedback diagram, I can write the reflected impedance in the dependent source,

$$Z_{2,1} = \frac{sMi_2}{i_1} = \frac{\omega^2 M^2}{\left(R_2 + \frac{Z_{0,2}^2}{R_L}\right)}. \quad (4.10)$$

The same current,  $i_1$ , flows through both elements, and I can write the fraction of energy dissipated in the dependent source as a voltage divider using Equations 4.3, 4.4 and 4.8,

$$\eta_k = \frac{P_{sMi_2}}{P_{IN}} = \frac{i_1^2 Z_{2,1}}{i_1^2 Z_1 + i_1^2 Z_{2,1}} = \frac{Z_1 L(s)}{Z_1 - Z_1 L(s)} = \frac{k^2 Q_1 Q'_2}{1 + k^2 Q_1 Q'_2} \quad (4.11)$$

Typically the unloaded secondary circuit can have a high quality factor meaning that overall quality factor  $Q'_2$  is dominated by the quality factor of the load  $Q_L = \omega R_L C_2$ . Equation 4.11 indicates the need to maximize the geometric coupling factor,  $k$ , quality factor of the primary circuit,  $Q_1$ , and the loaded quality factor of the secondary circuit,  $Q'_2$ , to achieve minimum dissipation in the primary coil's resistance. The equation also illustrates that above the critical coupling factor,  $k_{crit}$ , the primary-secondary coupling efficiency increases from 0.5 and begins to approach 1. From the Nyquist diagram for  $L'(s)$  in Figure 4-5, we can see that the maximum value of  $|L'(s)|$  is  $Q_1 Q'_2$ . At this maximum point, I can operate at or above  $k = k_c$  to have a coupling efficiency between the primary and secondary greater than 50%.

### Energy Dissipation in the Secondary Circuit

The energy coupled to the secondary circuit is dissipated in both the parasitic element,  $R_2$ , and the load network, represented in this linear model by  $R_{L,ac}$ . At resonance, writing the fraction of power delivered to the load element,

$$\eta_2 = \frac{P_L}{P_2} = \frac{Q_2}{Q_2 + Q_L}. \quad (4.12)$$

Equation 4.12 represents the energy divider relationship during the waveform cycle between the lossy elements,  $R_2$  and  $R_{L,ac}$ . Equation 4.12 delivers maximum energy to the load when the effective  $Q$  of the load network  $Q_L = \omega R_{L,ac} C_2$ , is minimized.

From Equation 4.11, the primary-secondary coupling efficiency,  $\eta_k$ , increases as  $Q_L$  is increased since  $Q'_2 = (Q_2 Q_L / (Q_2 + Q_L))$ ; from Equation 4.12, the secondary efficiency decreases as  $Q_L$  is increased. Thus, there is an optimum  $Q_L$  or equivalently, an optimal load  $R_{L,ac}$ , at which the overall energy efficiency is optimized.

### Optimal Loading Condition

The net energy efficiency is given by

$$\eta_2 \eta_k = \left( \frac{k^2 Q_1 Q'_2}{1 + k^2 Q_1 Q'_2} \right) \left( \frac{Q_2}{Q_2 + Q_L} \right), \quad (4.13)$$

By differentiating Equation 4.13 w.r.t.  $Q_L$ , I find an optimal loading condition at which the energy efficiency is maximized,

$$Q_{L,opt} = \frac{1}{k} \sqrt{\frac{Q_2}{Q_1}}. \quad (4.14)$$

At this optimum, the maximum achievable efficiency can be written in terms of the coupling factor and unloaded quality factors of the coils,  $Q_1$  and  $Q_2$ .

$$\eta_{MAX} = \frac{k^2 Q_1 Q_2}{(k Q_1 + 1)(k Q_2 + 1)}. \quad (4.15)$$

This form is more practical than writing a full solution of the losses in each resistive element and summing them as has been done previously [62].

Using values of experimental components listed in Table 4.1, and the experimental setup shown in Figure 4-6 and described in its caption, I obtained measurements of the RF link that illustrate the theoretical effects discussed above. Figure 4-7a reveals the frequency transfer functions of coupled resonators as the distance between the primary and secondary is varied. After the critical coupling distance (or equivalently after the critical coupling  $k_c$ ), where the voltage transfer function is maximized, there

Table 4.1: Efficiency Test Setup Parameters

Parameter	Notes
Output Power Level $P_{R_{L,ac}}$	4mW
Operating Frequency $f$	$\simeq 4.5\text{MHz}$
Coil Separation Distance $d$	$1\text{mm} - 30\text{mm}$
Class-E Power nFET	Fairchild NDS351 $R_{DS,on} \simeq 0.6\Omega$ for $V_{GS,on} = 3V$
$L_1$	10 turns of 32 gauge $r = 15\text{mm}$ $3.2\mu\text{H}$ with $Q_1 \simeq 70$
$C_1$ $C_S$	150pF 60pF
$L_2$	15 turns of 32 gauge $r = 15\text{mm}$ $4\mu\text{H}$ with $Q_2 \simeq 70$
$C_2$	220pF
$L_{RFC}$	Coilcraft 1812PS-223KL $L_{RFC} = 22\mu\text{H}$

are two frequency peaks with the lower frequency peak having higher Q and the higher-frequency peak having lower Q in accord with the root-locus predictions of Figure 4-4. Figure 4-7b shows that the voltage peak at resonance is non-monotonic and peaks at the critical coupling  $k_c \approx 0.1$ . Figure 4-8 shows the results of the overall power transfer efficiency (ignoring the Class E amplifier and rectifiers for now) for four separation distances. Note that the peak efficiency shifts to lower load resistance as the coils are moved closer together in accord with the theoretical predictions of Equation 4.14.

## 4.2 System Design

The power driver, inductive link, secondary circuit, and rectifier, each contribute to wasted power. The overall efficiency of the power system is the product of the power-processing stages, including the driver efficiency,  $\eta_{driver}$  and the rectifier efficiency  $\eta_{rect}$ . The overall efficiency is just the effect of all of these stages on the input power,  $\eta_{total} = \eta_{driver}\eta_k\eta_2\eta_{rect}$ .

Equation 4.15 predicts that the best unloaded quality factor for both primary and secondary coils maximizes the asymptotic efficiency of the link. Coils generally

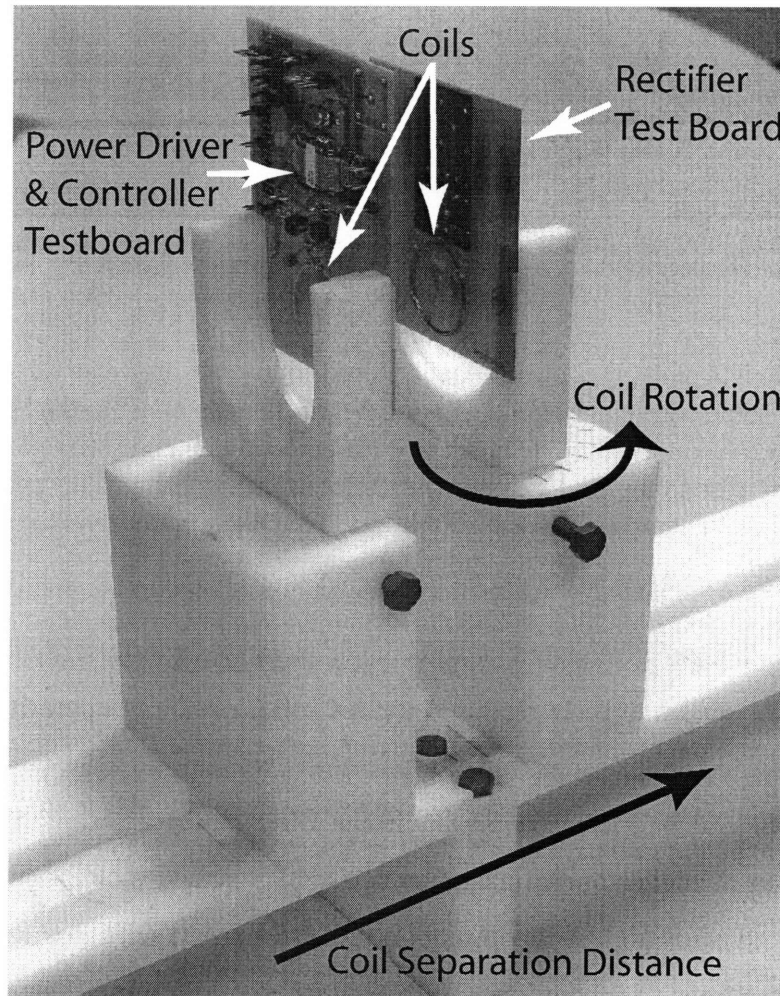


Figure 4-6: The test setup used for inductive power transfer system tests is shown. The coil separation can be adjusted and measured with millimeter accuracy. Coil rotation can also be explored for both the primary and secondary coils. The electronic boards are glued to Delrin scaffolding with Teflon screws used to bind the various portions of the scaffold.

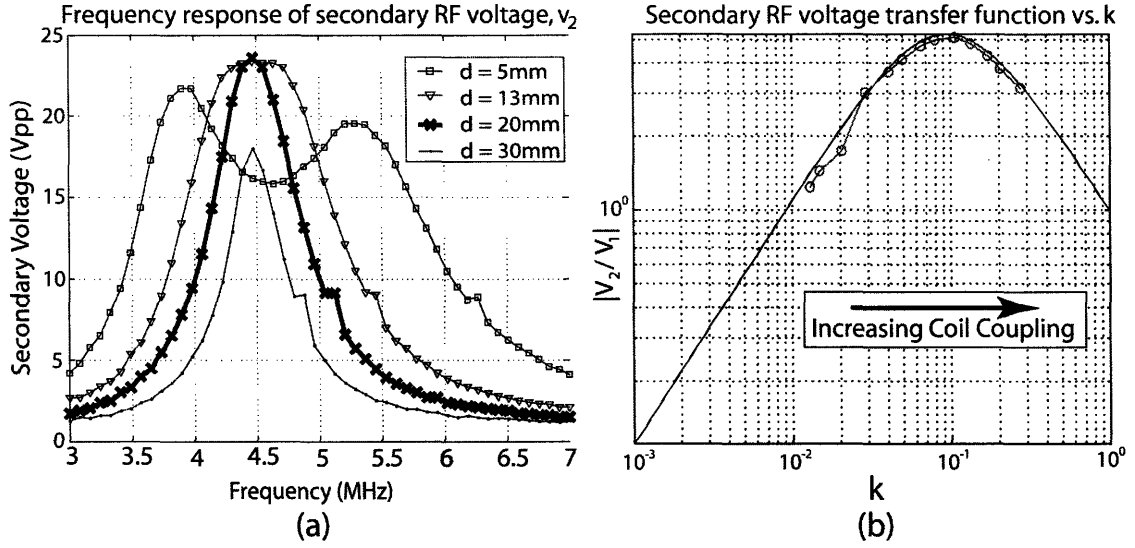


Figure 4-7: The left plot (a) shows how the closed-loop poles move as the coil distance is changed. At some coil separation, the poles begin to move apart and a low-frequency high-Q and high-frequency low-Q peak are observed. The right (b) plot shows the voltage peak at resonance as I change the coil coupling factor. The peak occurs at roughly  $k_c \sim 0.1$ .

have better  $Q$  at higher frequency  $\omega$  since their electromagnetic skin-effect resistive losses scale like  $\sqrt{\omega}$  while their reactance scales like  $\omega$ . A large operating frequency does however, lead to more sensitivity to parasitics, increased tissue absorption, and increased losses and or increased power in the Class E drivers that require better timing precision at higher operating frequencies. The presence of the high dielectric tissue of the body surrounding the implant can also lower the self-resonance frequency of the coil due to inter-turn coupling. With these tradeoffs in mind, I chose to operate at 6.78MHz, an unlicensed ISM band. I used multi-stranded Litz wire for the coils. Such wire mitigates skin-loss resistive effects by accumulating the increased skin-effect circumferential area available in each strand of wire rather than relying on the skin-effect circumferential area available in just one strand. In this operating frequency band, I can obtain inductors from  $1\mu H$  to  $15\mu H$  and quality factors of 80 – 150.

More details on the influence of the number of turns, coil separation, and coil misalignment on  $k$  can be found in [65]. To give a sense of the range of coupling factors for the coils in my system, a set of measurements for  $k$  are shown in Figure

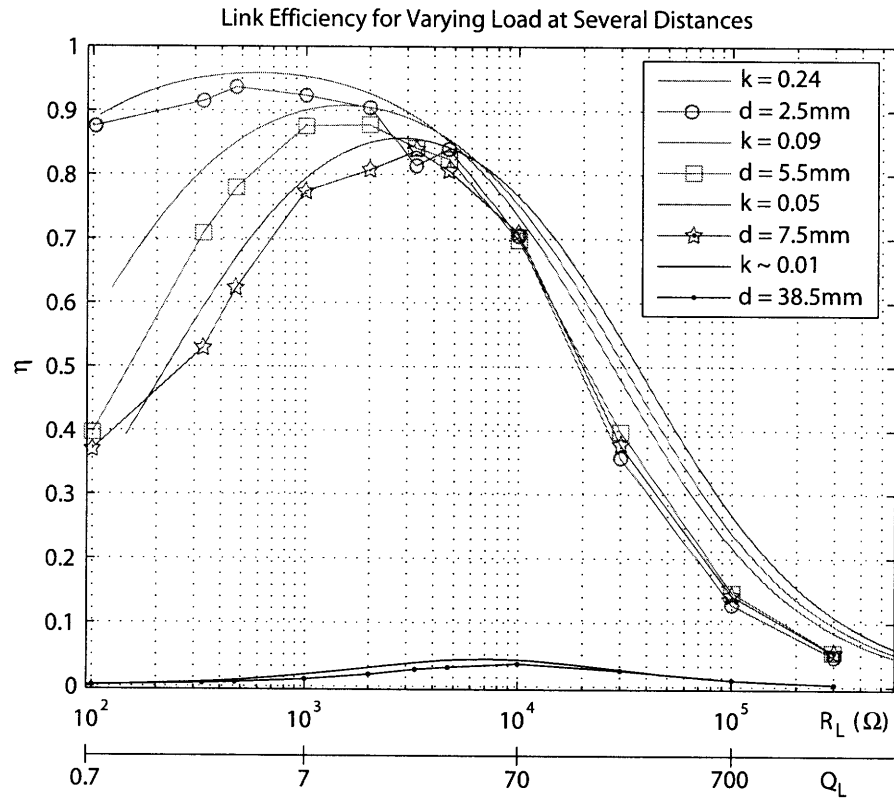


Figure 4-8: Efficiency of power transfer between coupled resonators for varying loading. The data I show were produced by ignoring switching losses in a discrete Class-E amplifier implementation.

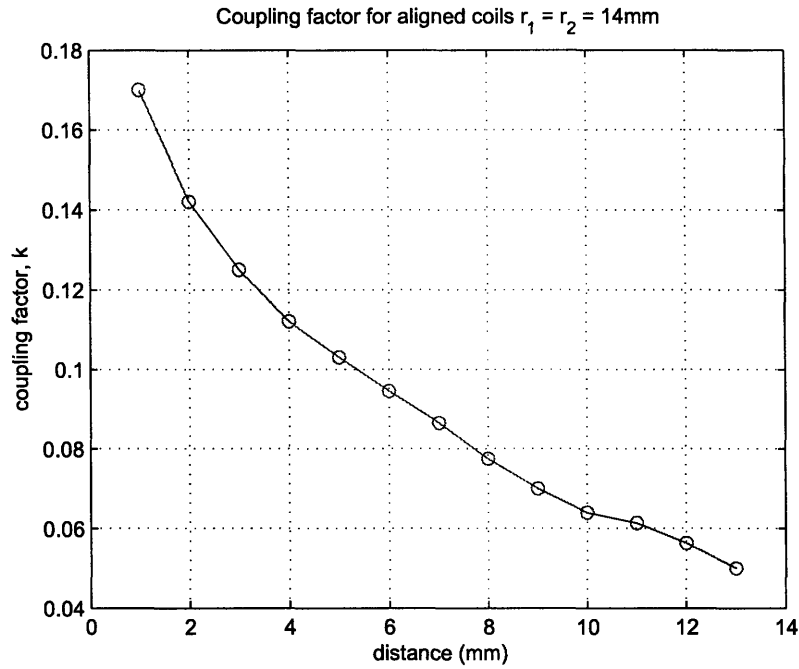


Figure 4-9: The coupling factor  $k$  for coils of radius 14mm are shown. These measurements were taken using the test setup shown in Figure 4-6.

4-9.

My design procedure begins with the inductive link and secondary circuit, as these are typically the most difficult to maximize. Then the design of the power driver and rectifier follow. My design is based on the following steps:

1. From the given load that one is required to drive in the secondary, and the mean expected  $k$ , design the secondary circuit for achieving optimal overall efficiency from Equations 4.14 and 4.15, and to maintain resonance at the desired operating frequency.
2. Choose a desired primary-secondary voltage gain of the link and implement it by choosing appropriate element values in the primary.
3. Design the power driver and rectifier circuits to be as efficient as possible by optimizing their design to yield minimum loss.



Table 4.2: Secondary Resonator Design

Parameter	Notes
$R_{L,ac}$	$2.5k\Omega$
$C_2$	93pF Mica $Q \sim 400$
Rectifier Diode, $D$	$2 \times$ HBAT54C Schottky diode $C_{par} \simeq 13pF$
$C_{2,total}$	119pF
$L_2$	8 turns of 22-strand Litz wire $r = 15mm$ $4.7\mu H$ with $Q \sim 140$
Unloaded $Q_2$	90
$Q_L$	12.6

#### 4.2.1 Resonator Design – Load Design

From the limitations on the physical size of the implanted and external coils, I can find the range of coupling factors for the operation of the system. The range of coupling factors can be reduced with intentionally misaligned coils [66], at the expense of peak efficiency. In many transcutaneous bionic implants, the skin-flap thickness,  $d$ , can vary from 1mm – 10mm. The implanted and external coils are chosen to have a radius of 14mm. This size and range of separations gives a range of coupling factors  $0.04 < k < 0.17$ . As the 6mm condition is the most common, I have chosen the coupling factor of 0.084 as the optimal coupling factor. Therefore, the optimal loading quality factor is  $Q_{L,opt} \simeq 12$ .

The electrode stimulation circuits present an effective load resistance to each of the rectified supply voltage nodes,  $+V_{RECT}$ , and  $-V_{RECT}$ , of  $10k\Omega$ . For both rectifiers in parallel, the effective  $ac$  resistance load,  $R_{L,ac} = 2.5k\Omega$ . Now, with the operating frequency and the load quality factor chosen, this constrains the choice of secondary capacitance and inductance. Note that the effective capacitance at the resonator node,  $v_2$ , must account for the capacitance due to the diodes, as well as parasitic capacitance due to the self-resonance of the coil. For a robust implanted design, the coil capacitance must be much smaller than the explicit capacitance at the node  $C_2$ , to prevent tuning shifts when the unit is implanted under tissue. The final secondary circuit design is summarized in Table 4.2.

With the secondary network chosen, I can turn to the design of the primary. The

voltage gain between the primary and secondary circuits can be scaled by choosing the primary inductance  $L_1$  w.r.t. the secondary inductance  $L_2$ : The voltage gain at the critical coupling when  $k_{crit}^2 |L(j\omega_n)| = 1$ , is the maximum possible gain obtainable. Its value is easily found by substituting  $M = k_{crit} \sqrt{L_1 L_2}$ ,  $k_{crit}^2 Q_1 Q'_2 = 1$ ,  $L_1 C_1 = L_2 C_2 = 1/\omega_n^2$ , and  $L(s) = -1$  in Equation 4.7 with  $\omega_n C_2$  assumed much greater than  $1/R_{L,ac}$  (i.e.,  $Q_L$  is at least greater than 10). It is found to be

$$\left(\frac{v_2}{v_1}\right)_{MAX} = \frac{\sqrt{Q_1 Q'_2}}{2} \sqrt{\frac{L_2}{L_1}}. \quad (4.16)$$

For my system, I chose a primary inductance of  $L_1 = 6.5\mu H$  to reduce the gain due to the high quality factor of the resonators. With the choice of  $L_1$ , the value of  $C_1$  is chosen such that  $L_1$  and  $C_1$  resonate at  $\omega_n$ .

### 4.2.2 Driver Design

When designing power amplifiers to drive the primary in low-power RF links, there are three considerations: First, the output resistance of the drive circuitry must not reduce the effective quality factor of the primary circuit greatly to maintain the asymptotic efficiency performance derived in Equation 4.15. Second, the driver should be resilient to changes in the load – the reflected load from the secondary circuit can constantly change the primary resonator's damping characteristics. Finally, complex techniques for reducing capacitance switching at control terminals in a power amplifier are too costly in milliwatt systems like ours and are to be avoided. A design that fulfills these requirements is described below.

Figure 4-10 shows a Class-E power amplifier: A single switch  $M$  is used to periodically toggle between fluxing up an inductor,  $L_{RFC}$ , or switching the current in the inductor to the output network at the drain node,  $v_d$ . The resultant square wave harmonics are filtered by the resonant driven network. With careful choosing of the load  $C_S$  w.r.t. to the dynamics and parameters of the driven primary network, this topology can minimize  $f C_S v_d^2$  switching losses in  $M$ , by only turning  $M$  on when  $v_d$  is near ground [67].

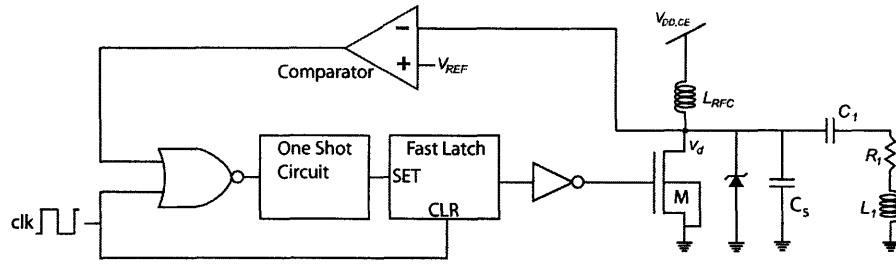


Figure 4-10: A switching power driver (Class-E) is shown with the primary circuit and a one-shot control loop. The Class-E supply voltage,  $V_{DD,CE}$ , controls the power level, while the clock, comparator, NOR gate, one-shot circuit and latch control the gate drive timing.

The damping seen in the driven primary changes due to variations in the reflected impedance from the secondary caused by variations in coupling. To adapt to these changes, I built a simple one-shot feedback controller, shown as control blocks on the left half of Figure 4-10. The drive circuit is triggered by a fixed clock which resets the gate drive signal through a dynamic latch turning the power switch  $M$  off when the clock goes low. The current from  $L_{RFC}$  is then directed onto  $C_S$  and the primary network. When the resonator voltage drops near ground again due to the resonant behavior of the driven network the comparator triggers and turns on the power switch through the NOR gate, a pulsatile one-shot, and fast latch. If the comparator signal has not arrived by the end of the clock cycle, then the high-going clock will turn on  $M$ . Thus, the controller achieves fixed-frequency operation set by the clock, but adapts to changes in the driven network that speed up the return of  $v_d$  to ground. The comparator is implemented as a simple ratioed inverter and shown in Figure 4-11.

### Optimal device sizing of the switching transistor in the Class E amplifier

When the switching transistor  $M$  in Figure 4-10 is turned on, it conducts current flowing from  $L_{RFC}$  and from the primary resonator. A large  $W/L$  for the switching transistor  $M$  in Figure 4-10 reduces its on resistance,  $R_{DS,on}$ . A low  $R_{DS,on}$  is important for ensuring that the quality factor of the driven primary resonator is not degraded greatly; a large  $W/L$  also minimizes the  $I_{RFC}^2 R_{DS,on}$  loss, although this loss



0.5 $\mu$ m. Such a transistor is implemented with many parallel fingers on a chip.

During the time when the FET  $M$  is turned off, the drain voltage pulse can reach high voltage values. The integrated devices have a breakdown voltage of 11V. To avoid breaking down these devices, the resistance seen in the primary by the Class-E driver must be low enough to not cause breakdown or the Class-E driver must be run with  $V_{DD,CE}$  in Figure 4-10 low enough to not cause breakdown. In addition, an off-chip Schottky diode protects  $v_d$  from under voltages below ground. At these low power levels, the effective magnetic field strength is low enough such that regulatory issues are not a big concern.

### 4.3 Measured Performance

I fabricated a power-system chip on AMI's 0.5 $\mu$ m SCMOS process offered by MOSIS. Figure 4-12 shows the die which includes two sizes of power switches, and includes independent gate drivers and controllers, PTAT comparator biasing, a crystal clock generator, and a feed-forward data path described in Chapter 5. Testing was done for a 1.8V digital supply voltage. The controller comparator, shown in Figure 4-11, was biased with 28 $\mu$ A and sized to minimize delay. Including wasted biasing power, the comparator consumes 56 $\mu$ W of power. The gate driver and remaining control circuits consume 48 $\mu$ W from the supply. All these dissipations are added in my computations of the final efficiency so that it is as accurate is possible. Table 4.3 shows our final measured parameters for the rest of the system.

The primary coil,  $L_1$ , had an intrinsic quality factor of over 100. However, the power switch in the Class-E amplifier contributes to the effective series loss in the primary significantly, such that

$$Q_{1,eff} = \frac{\omega L_1}{R_1 + R_{DS,on}}. \quad (4.18)$$

Since  $R_{DS,on}$  was found to be 5 $\Omega$ , it reduced the primary quality factor to 35. Table 4.4 summarizes my final measured performance numbers including this effect. Figure

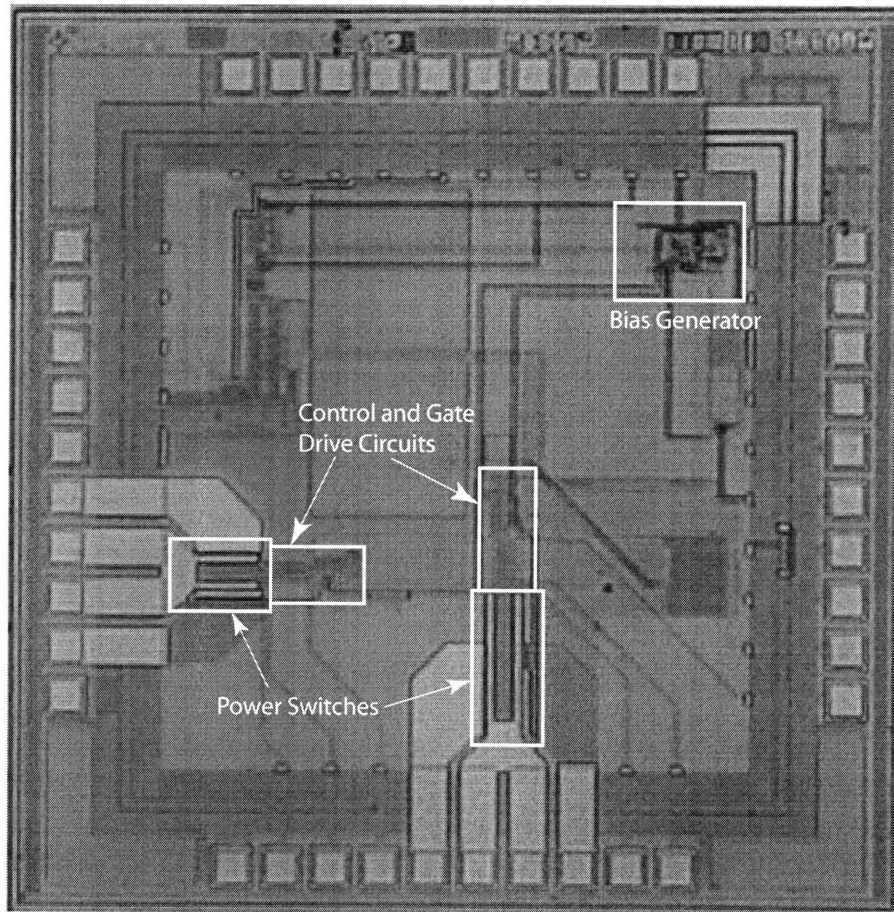


Figure 4-12: Die photograph of the  $0.5\mu\text{m}$  power systems chip. This chip includes two power switches and two independent controllers. A clock generator, for off-chip crystals, as well as a feed-forward data system (not discussed in this chapter) are also included on the chip.

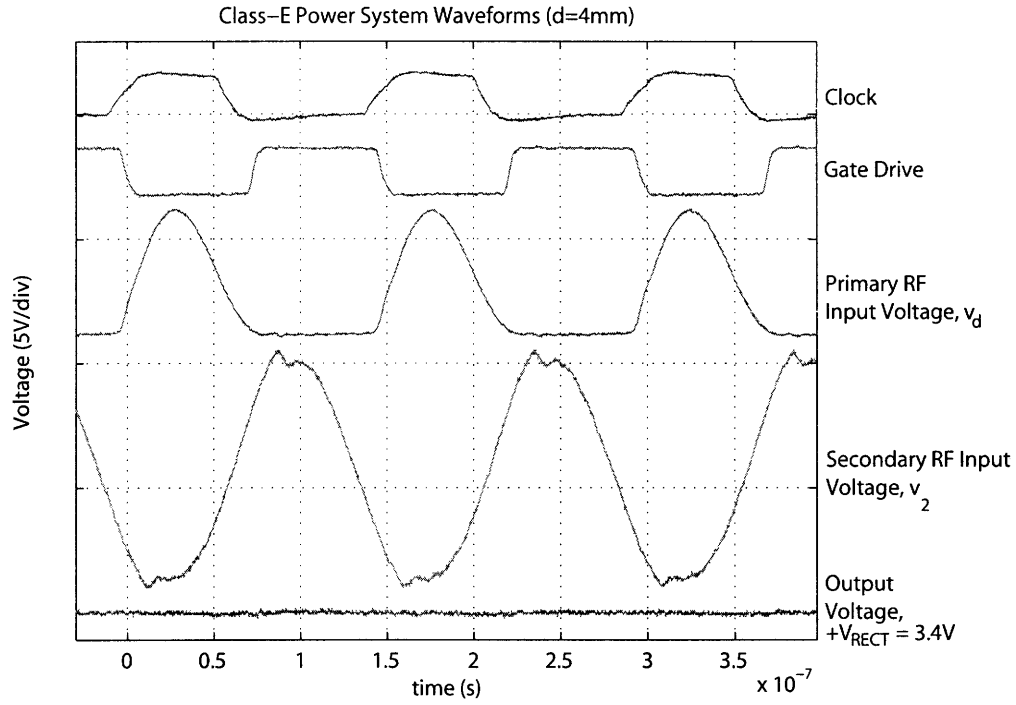


Figure 4-13: System waveforms, including the clock, gate-driver signal, Class-E drain voltage  $v_d$ , secondary voltage  $v_2$ , and rectified voltage  $V_{RECT}$  are shown for a 4mm coil separation condition.

4-13 shows the basic waveforms of the Class E driver. Figure 4-14 illustrates that my clocked one-shot strategy is operating over a 1mm-10mm range of coil separations.

Figure 4-15 shows the variation of rectified output voltage over a range of coil separations. For all coupling cases, there is less than 16% difference in the minimum and maximum voltages. Thus, my design, which targets efficiency rather than critical coupling, is nevertheless robust in its voltage-transfer characteristic to changes in link coupling.

In future work, a feedback system which measures the appropriate primary-secondary voltage-power relationship can be implemented without much power. Such a system could use 4 bits to set the voltage range for the factor-of-10 variation in power levels from 1mW – 10mW. A range of primary class-E voltages from only 0.6V – 2.5V can provide the needed range of power to the secondary over all possible separation conditions.

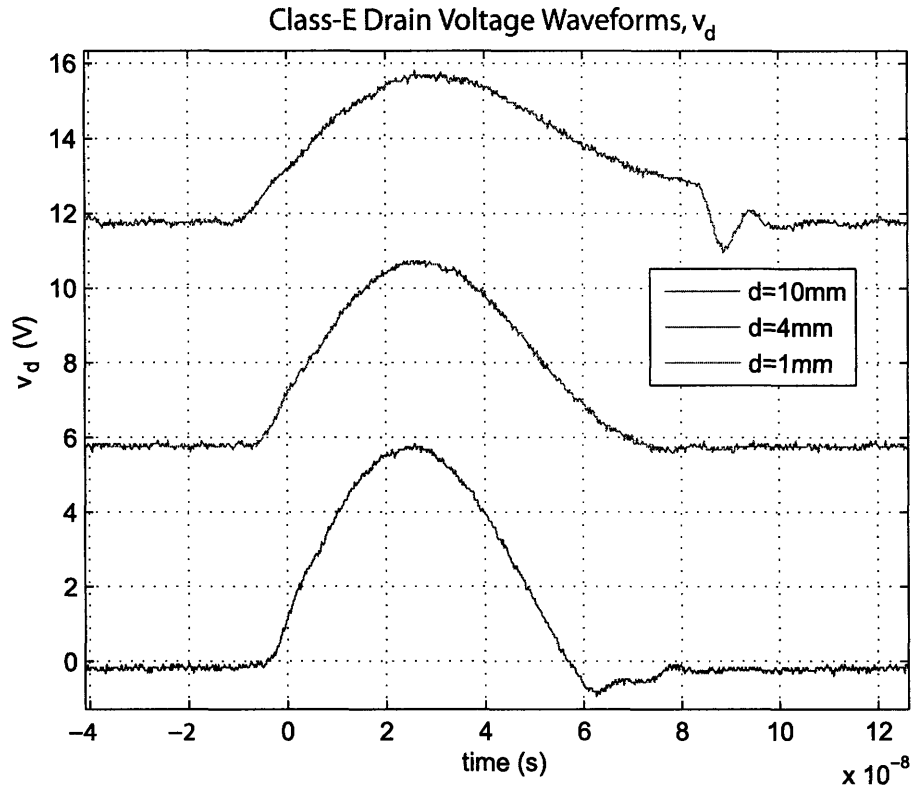


Figure 4-14: Three cases are shown for the Class-E drain voltage  $v_d$ . Note that the switch timing has adapted slightly to reduce the amount of  $fC_s v_d^2$  wasted power under the 1mm and 10mm conditions. Furthermore, the action of the protection diode can be seen in the  $d = 10\text{mm}$  case where the drain voltage has dropped below ground.



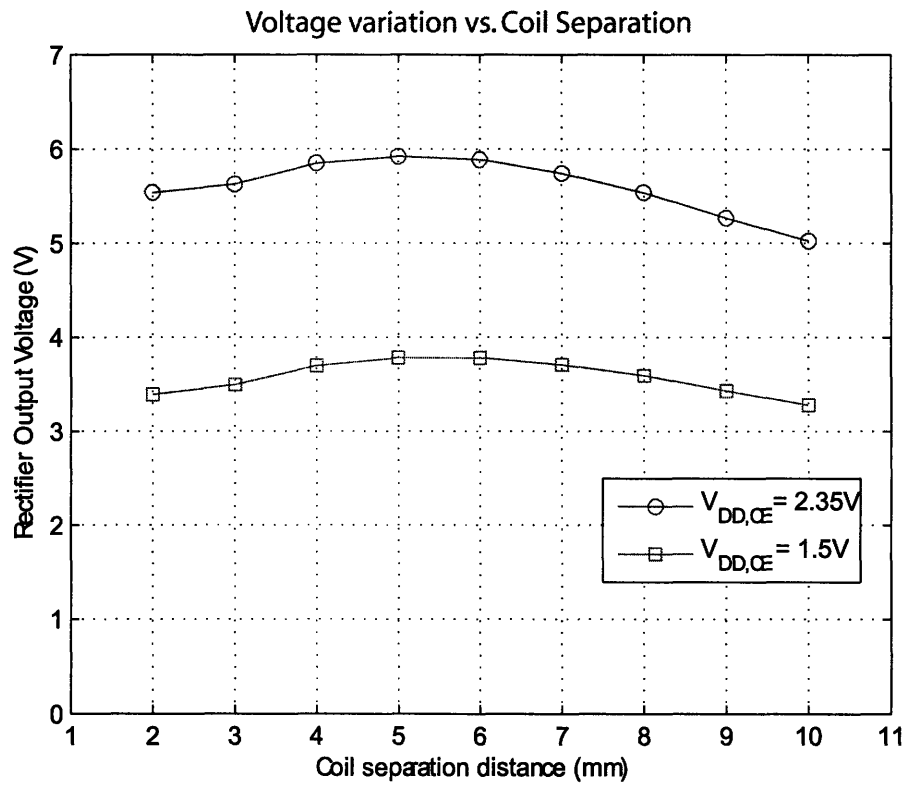


Figure 4-15: Variation in the rectified output voltage is shown for two power driver voltage levels. The rectified voltage variation is less than 16% for all cases.

### 4.3.1 Efficiency

I tested the overall efficiency for a range of distances and power levels suitable for the application. Figure 4-16 compares my measured efficiency with theoretical predictions. The top trace indicates the theoretical performance possible if the load is adapted for each coupling factor, i.e., Equation 4.15. The dashed trace shows the theoretical performance for a fixed  $Q_{L,opt} \simeq 12$ , the experimental situation, and for which Equation 4.13 is predictive. As can be seen, the agreement with theory is fairly good. The 1mW characteristic deviates more from theory than the 10mW characteristic because the fixed power used by the controller and gate drive power are a more significant fraction of the overall power.

To examine deviations of experiment from theory more closely, Figure 4-17 breaks down the efficiency of the various components of the system. These *efficiencies* were determined from measurements of the wasted power, the input power, and output power at the secondary. At the lowest power operating level, rectifier and gate-switching losses contribute the most because these losses do not scale with power level like efficiencies in linear portions of the system, e.g., the primary-secondary coupling.

My system delivers 10mW at typical coil separations with 61% efficiencies, in excellent agreement with theoretical predictions. Note that a higher value of  $Q_{L,opt}$  would improve efficiency for low  $k$  as Figure 4-16 shows or Equation 4.14 predicts. The  $5\Omega$  series resistance of the power switch degrades efficiency due to the reduction in the quality factor of the primary. Using Equation 4.15 at  $k = 0.09$ , and a redesigned value for  $R_{DS,on} = 2\Omega$ , the asymptotic efficiency can be as high as 85%. A more thorough analysis of the losses in the amplifier, including a more detailed tradeoff of conduction and switching losses is presented in Appendix B.

I obtained efficiency measurements with a bag of saltwater as well as a slab of Delrin between the primary and secondary coil. The measurements indicated a slight shift in resonance frequency which degraded my efficiency by 2% to 3%. The robustness of my design to such effects is because an explicitly large  $C_2$  in the secondary

Table 4.3: Final System Specifications

Parameter	Notes
Output Power Level $P_{RL,dc}$	1mW – 10mW + $V_{RECT}$ , $-V_{RECT}$ with $R_{L,dc} = 10k\Omega$ each
Operating Frequency $f$	6.785MHz (on-chip generator w/ off-chip crystal)
Coil Separation Distance $d$	1mm – 10mm
Class-E nFET	100 fingers $\times 12\mu m \times 0.5\mu m$ $C_{gate} \sim 2.1pF$
Class-E Supply Voltage, $V_{DD,CE}$	0.6V – 2.5V
$L_1$	10 turns of 22-strand Litz wire $r = 15mm$ $6.5\mu H$ with $Q_1 \sim 94$
$C_1$ $C_S$	1000pF Mica 30pF
$L_2$	8 turns of 22-strand Litz wire $r = 15mm$ $4.7\mu H$ with $Q_2 \sim 90$
$C_2$	93pF
Rectifier Diode, $D$	$2 \times$ HBAT54C Schottky diode $C_{par} \simeq 13pF$
$L_{RFC}$	Coilcraft 1812PS-223KL $L_{RFC} = 22\mu H$

that dominates over stray capacitance and self-resonance effects in the coils.

## 4.4 Summary

I have used a feedback viewpoint to add geometric insight to the design of RF power links. My design approach focused around the choice of an efficiency-maximizing load for an expected mean separation between primary and secondary coils. The approach also yields voltage-transfer functions that are fairly robust to changes in coil coupling parameters. I used these techniques to build an RF power link for use at 1mW-10mW load power-consumption levels and for 1mm-10mm coil separations. At such low power levels, rectifier losses and Class-E power amplifier losses contribute significantly to the inefficiency of the overall system. I described a novel integrated Class-E power amplifier design that used a simple control strategy to minimize such losses. At 10mW load power consumption, I measured overall link efficiencies of 74% and 54% at 1mm and 10mm coil separations respectively, in good agreement with

Table 4.4: Final System Performance

Component	Performance @ $V_{DD} = 1.8V$
Gate Driver	$46\mu W$
Gate Switching Controller	$56\mu W$
Power Switch, $M$	$R_{DS,on} \simeq 5\Omega$
$Q_{1,eff}$	35
$Q_2$	90
$\eta_{total}$ @ 1mW	66% @ $d = 1mm$ 62% @ $d = 6mm$ 51% @ $d = 10mm$
$\eta_{total}$ @ 10mW	74% @ $d = 1mm$ 66% @ $d = 6mm$ 54% @ $d = 10mm$

System Efficiency:  $f = 6.78MHz$ ,  $V_{DD} = 1.8V$ ,  $Q_1 = 35$ ,  $Q_2 = 90$

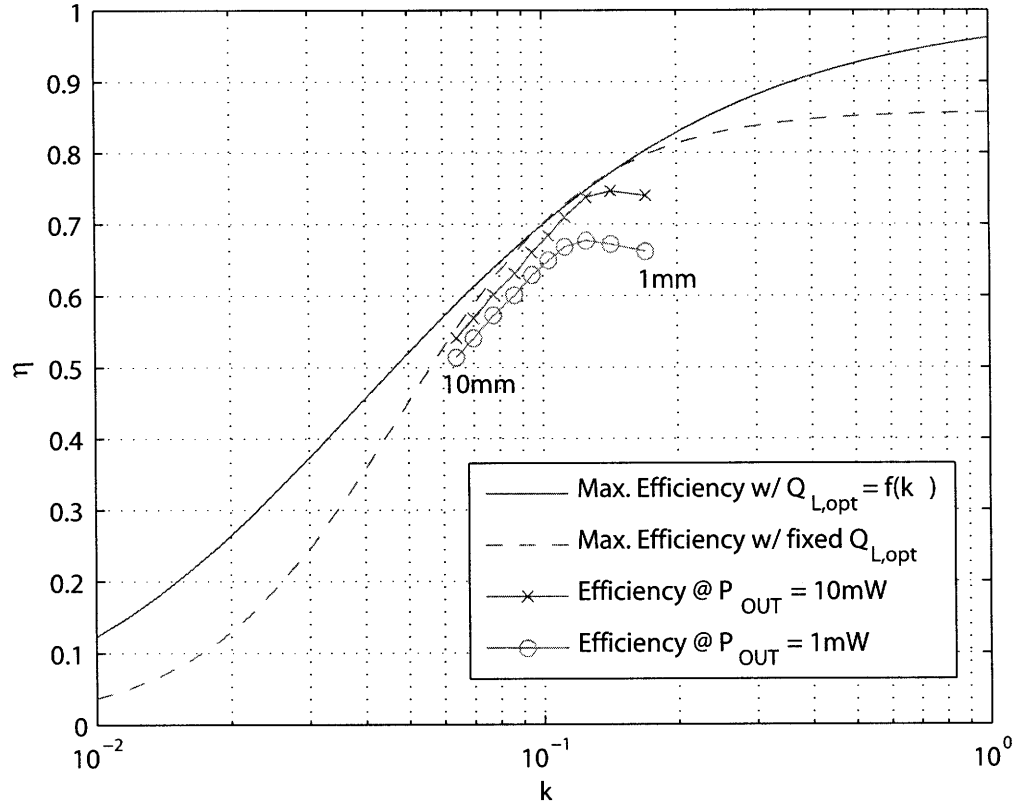


Figure 4-16: A comparison between the asymptotically efficient coupled resonator power transfer system ( $Q_1 = 35, Q_2 = 90$ ) is shown with my system. The top curve indicates the maximum possible efficiency for an adapting load condition (Equation 4.15). The dashed theory curve indicates efficiency for the fixed loading condition,  $Q_{L,opt}$ , (Equation 4.13). My system performance is shown for 10mW and 1mW operation.

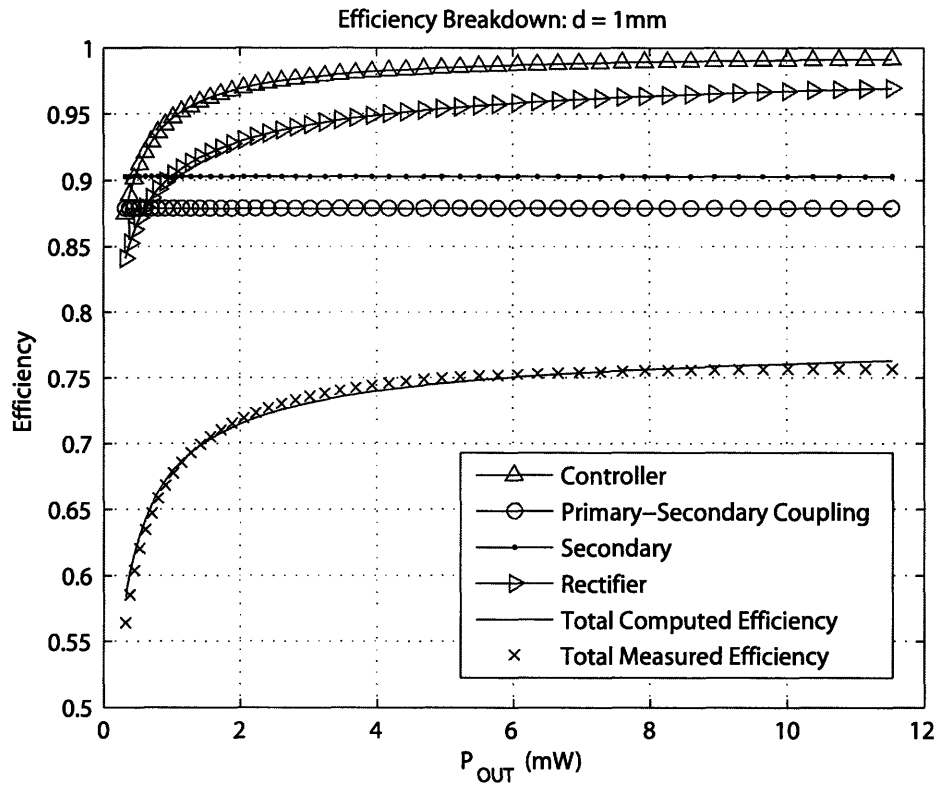


Figure 4-17: A plot of the efficiency is shown for a sweep in the power level by changing the class-E supply voltage. The efficiency of each mechanism is shown for comparison. At low power levels, controller power and losses in the rectifier contribute most to inefficiency of the system.

my theoretical predictions of the link's efficiency. At 1mW load power consumption, I measured link efficiencies of 67% and 51% at 1mm and 10mm coil separations respectively, also in good accord with theoretical predictions. In both cases, the link's rectified output DC voltage varied by less than 16 percent over link distances that ranged from 2mm to 10mm.

Now that I have demonstrated key building blocks of the cochlear implant system, I will describe an full system that takes advantage of each of the systems described in the previous chapters.

## Chapter 5

# A Low-Power Transcutaneous Cochlear Implant System With Feedforward Power Control

To this point, this thesis has described some individual subsystems of a bionic ear. Each of these parts, including the front-end, compression AGC, and power transfer system are important to the power consumption and performance of an implant. Over the years cochlear implants have evolved from a simple device that connected the front-end output directly to a one-electrode stimulation array, to multielectrode devices with complex time-dependent neural coding strategies [2].

In Chapter 1 I introduced the idea of a transcutaneous cochlear implant. Figure 1-2 showed how the systems in a modern cochlear implant are organized. This chapter will describe a complete bionic ear system from microphone to the power delivered to the electrode driver array. Two key components of the complete system have been ignored. These are the data transfer system, and the current stimulator chip. Data links across thin layers of skin can achieve as little as  $2\text{nJ}$  per bit [11]. For our system the data link could be included for less than  $10\mu\text{W}$ . The current stimulator chip is not critical to proving the value of my system design because the power that it consumes is being accounted for in a model load.

This chapter is organized as follows: Section 5.1 describes a low-power bionic

ear processing chip which performs the programmable analog channel-wise signal processing. Section 5.2 describes the overall system board and a feedforward power controller. Section 5.3 describes the results for both fixed and adaptive electrode power schemes. In Section 5.4 I summarize the experimental results for the bionic ear board. Finally, I discuss the lessons and contributions of this thesis in Section 5.5.

## **5.1 Analog Bionic Ear Processing (ABEP) System**

Current implant speech-processing strategies are based on a mel cepstrum filter bank with 8–20 channels. The mel scale maps frequencies to a scale that is perceptually linear for human listeners [42]. A mel filter bank uses linearly spaced center frequencies up to 1kHz and logarithmically spaced center frequencies above 1kHz. The log energy of each of these channels is then further processed to stimulate the 8–20 electrodes to stimulate the auditory nerve. Using significantly more electrodes is often not useful because the electrodes interact with each other due to current spreading in the cochlear tissue.

A 16-channel implant processing system, designed by the AVBS team at MIT, and diagrammed in Figure 5-1, meets these signal processing needs with remarkably low power. I will describe how this was accomplished in general terms. More extensive details of the chip are presented in [6][36][41].

This section describes the parts of the bionic ear processor chip developed between 2002 and 2005 in the Analog VLSI and Biological Systems group at MIT. First, I describe how the front-end and gain control circuits are programmed and used in the cochlear implant processing chip. Second, an outline of the channel programming and operation is presented.

### **5.1.1 Front-end Signal Processing**

First, the low-noise preamplifier described in Chapter 2 amplifies signals from a low-power microphone or auxiliary inputs. Bias currents, generated from the current reference, were bypassed to the supplies to remove additional coupling pathways.



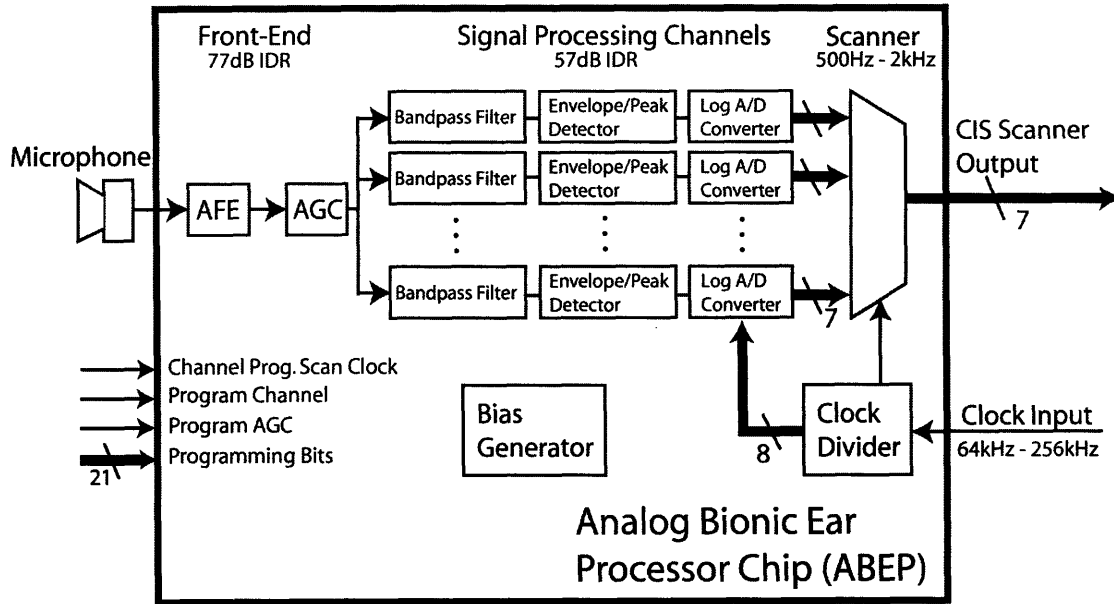


Figure 5-1: An analog bionic ear processor chip architecture is diagrammed. The signal path consists of a programmable front-end and 16 programmable channels. The bias generator connections to each of the analog blocks are not shown to avoid clutter on the figure.

Table 5.1: Programming variables in ABEP front-end and Single-loop AGC

Parameter	Number of Bits	Programming Range
Compression Ratio ( $\alpha$ )	4	1 – 1.67
Maximum Gain (Knee)	4	1 – 12
Attack Time-Constant	4	4ms – 50ms
Release Time-Constant	4	20ms – 280ms

Although the analog front-end is a single-ended circuit, the PSRR performance is quite good due to active supply filtering. To preserve this supply immunity as much as possible, a matched level shifting circuit is used to couple the audio signal and the reference for the next stage – the automatic gain control circuit.

A single-loop AGC, similar to the one described in Chapter 3, further amplifies the signal with programmable gain control parameters. Similar to the tested designs described previously, this integrated version has 16 programmable bits controlling parameters summarized in Table 5.1.

After the signal has been amplified and compressed to 57dB IDR, a buffer is used to drive the inputs to 16 channels. A buffer is needed because the input of each

channel is a capacitive attenuator load which can be modeled as an electrical load of approximately 1pF.

### 5.1.2 Programmable Processing Channel

This section describes the programmable channel in the bionic ear processing chip. First, the signal is bandpass filtered by a programmable Gm-C filter [72]. To shift the dynamic range of the standard diff-pair Gm-C topology to a larger voltage swing, a capacitive divider is used to attenuate the signal prior to filtering.

The envelope of this signal is then estimated by converting the filter output to a current, rectifying it and filtering this current in a current-mode filter with programmable asymmetric attack and release time constants [34]. The channel's logarithmic A/D converter has programmable calibration and sampling-rate parameters [73].

The output of the bionic ear processor uses a common electrode-stimulation strategy that applies current pulses to the electrodes in numerical order starting from the lowest frequency and finishing at the highest frequency. Called continuous interleaved sampling (CIS), this strategy ensures that no more than one electrode is being stimulated at a time by scanning the A/D channel output bits into a parallel data bus whose bits are timed with an output clock.

To program various on-chip parameters, current-mode DACs are biased from a PTAT reference circuit. To program each channel independently during patient calibration, a programming clock shifts parallel bits to each channel. Distributing the bias currents directly to each channel, instead of distributing gate voltages, reduces the effect of threshold voltage mismatch on the biasing. The programmable parameters for each channel are shown in Table 5.2.

To improve the robustness of this bionic ear processor with temperature, a constant- $g_m$  current reference circuit is included to bias all of the analog circuits. The current reference is designed to provide a current that is proportional to absolute temperature (PTAT), to compensate for the change in saturation current of all the devices on the chip.

Table 5.2: Programming variables in each ABEP channel

Parameter	Number of Bits	Programming Range
Bandpass filter center frequency	7	109Hz – 7054Hz
Bandpass filter Q	7	0.187 – 12.1
Envelope detector attack time-constant	2	1ms – 4ms
Envelope detector release time-constant	3	3ms – 24ms
Log-A/D minimum current reference	3	50pA – 400pA

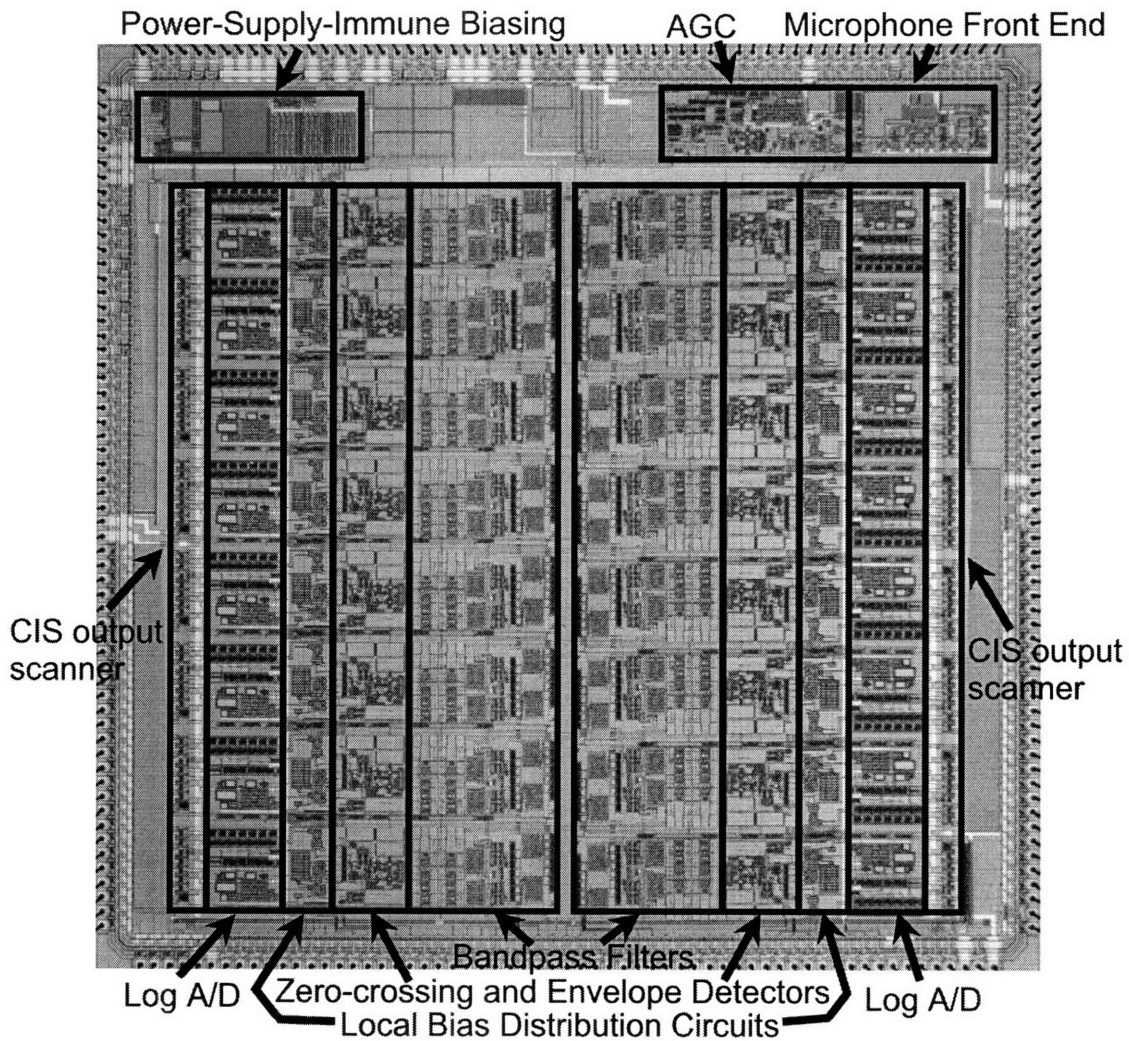


Figure 5-2: The analog bionic ear processing chip die photo shows each of the signal processing and biasing stages. This die is  $10\text{mm} \times 10\text{mm}$  and requires only four off-chip components to operate – an off-chip microphone and two gain-setting resistors are needed as well as a clock source. This chip operates from a 2.8V supply with only  $90\mu\text{A}$  of current.

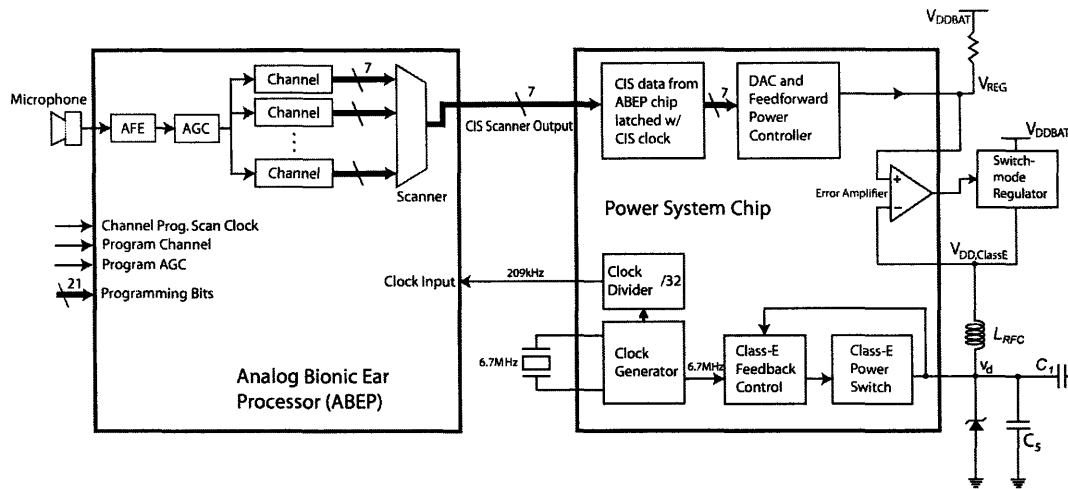


Figure 5-3: An outline of the transcutaneous implant architecture using the ABEP processor and power system chip. Clock generation for the power amplifier and the ABEP is done by the power system chip. The ABEP chip accepts audio input from microphones and auxiliary sources, programming bits from an external memory, and sends CIS output bits to the power system chip for feedforward programming of the just-needed power for the implanted unit.

The overall chip consumes  $90\mu A$  of power from a  $2.8V$  supply for a total power consumption of  $251\mu W$ . A die photograph of the chip is shown in Figure 5-2. The design was fabricated in the AMI MOSIS  $1.5\mu m$  BiCMOS process.

## 5.2 A Transcutaneous Bionic Ear Implant

To date, bionic ears have been designed with the microphone and signal processing on the outside of the body and stimulation underneath the skin. Any connection through the skin is avoided in implanted design to prevent infection for the patient. Access to the external signal processing components also gives transcutaneous implants greater flexibility for reconfiguration and updates without additional surgery. The implanted unit consumes power primarily to stimulate the electrodes with current pulses. Stimulation power can be anywhere from  $1mW$  to  $10mW$  depending on the design of the electrode array and the positioning of the array inside the cochlear tube.

The system architecture which I explored for a low-power transcutaneous implant

is diagrammed in Figure 5-3. First, audio inputs are processed by the channels and digitized as described above. The CIS outputs are then clocked sequentially into the power system chip registers. To minimize the power drawn outside the body I only want to deliver the power to the implant that is needed for this stimulation.

Because we know how much power is needed outside the body, it is possible to program the power level dynamically using the ABEP data stream. The feedforward power control circuit converts these bits into a current and performs a nonlinear mapping from the current to a needed supply control voltage,  $V_{REG}$ . The power delivered to the implanted secondary is modulated by then controlling the supply voltage of the class-E amplifier,  $V_{DD,ClassE}$ . This is done by using the  $V_{REG}$  voltage to control an off-chip switching regulator, the LTC3405A [74].

Also shown in Figure 5-3 are the clock generation and distribution blocks. The power system chip connects to an off-chip crystal reference at 6.75MHz to generate a clock for the power system and the bionic ear processor.

A two-chip solution of this type has a number of benefits. First, the low-noise analog circuits can be implemented on a separate die from high-current switching circuits. This helps to reduce pickup and interference which may not be entirely attenuated by the supply rejection techniques applied in the front-end circuits. Second, it is advantageous to have a more advanced process, with smaller minimum device lengths, available for the power system. Devices with high  $W/L$  ratios reduce the amount of gate-charge needed to realize a small on-resistance in power switching devices reducing both the conduction and switching losses.

### 5.2.1 Feedforward Power Control

The implanted unit rectifies power in the secondary resonator onto a supply capacitor,  $C_{RECT}$ . Charge for the electrode driver is drawn from this capacitance during stimulation. As I noted in Chapter 4, I can make an approximate linear model of the CIS electrode driver load by determining the voltage-current relationship for the entire electrode array. Using a simple electrode model with series resistance,  $R_E$ , and electrolyte capacitance,  $C_E$ , shown in Figure 5-4, I can write the needed internal

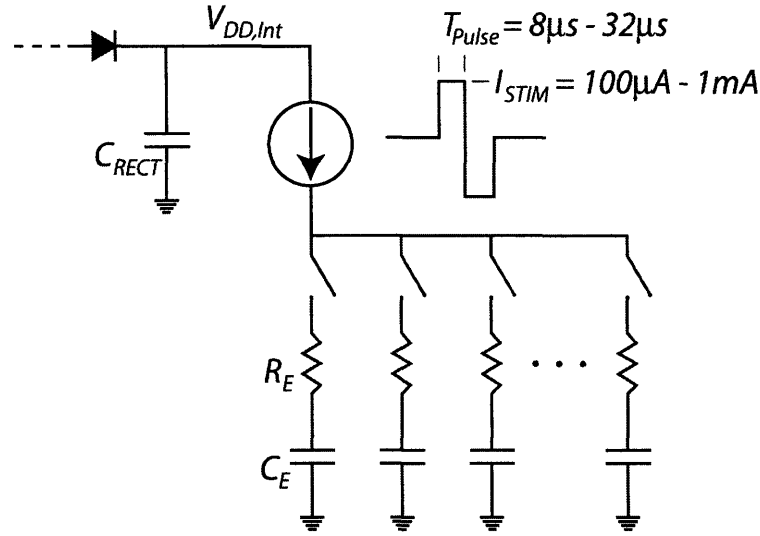


Figure 5-4: A simplified model of the internal electrical load is shown for a simple CIS stimulation strategy. An array of  $N$  electrodes is stimulated with a biphasic current pulses of length  $T_{Pulse} \times 2$ . Each electrode is stimulated with a repetition frequency of  $f_{CIS}$  and each pulse can have a range of current intensities at each electrode from  $100\mu A$  to  $1mA$ .

Table 5.3: Approximate CIS/Electrode Parameters

Parameter	Value
$N$	16
$I_{STIM}$	$100\mu A - 1mA$
$f_{CIS}$	2kHz
$T_{Pulse}$	$30\mu s$
$R_E$	$5k\Omega$
$C_E$	20nF

supply voltage,

$$V_{DD,Int} = I_{STIM} \left( \frac{T_{Pulse}}{C_E} + R_E \right) + V_{DS,Sat}. \quad (5.1)$$

Here,  $V_{DS,Sat}$  is the compliance voltage of the current source. The total current drawn from the internal supply is,

$$I_{Total} = I_{STIM} N f_{CIS} T_{Pulse}, \quad (5.2)$$

where  $N$  is the number of channels, and  $f_{CIS}$  is the stimulation frequency for each electrode.

To simplify my design, I write an approximate resistance for the stimulator load, from Equations 5.1 and 5.2, and using the range of parameters for the electrodes in Table 5.3. For these typical values I expect to see an effective load of  $7.5k\Omega - 12k\Omega$ . This resistance is largely insensitive to the stimulation current level because the more current is used, the higher the voltage on each electrode, meaning the overall network still acts as a linear element dissipating charge from the internal supply capacitor.

The supply capacitor,  $C_{RECT}$ , must be large enough to ensure that sufficient charge can be supplied during the current pulses without the voltage dipping below the driver compliance. During any given time period the maximum voltage needed for a set of stimulation currents  $\bar{I}$  is  $\max(\bar{I})R_L$ . Also, during this time-frame, the power needed in the stimulator is the sum of power consumptions due to each CIS stimulation event. Approximating the total power needed in the stimulator,

$$P_{stim} \simeq 2T_{Pulse} \sum_{j=1}^N V_{DD,Int} I_j = 2T_{Pulse} R_L \max(\bar{I}) \sum_{j=1}^N I_j. \quad (5.3)$$

A simple upper bound on this power consumption is,

$$P_{stim} \leq 2NT_{Pulse} \max(\bar{I})^2 R_L. \quad (5.4)$$

This may overestimate the power required in the implanted stimulator; however, it ensures that the drivers never run out of charge in the supply. Solving for the desired internal supply voltage function from Eq. 5.4,

$$V_{DD,int} \propto \sqrt{\max(\bar{I})} \quad (5.5)$$

Conceptually, the factor that decides the amount of charge needed is the average power in a given time window, not the peak current. So, although the range of power levels needed internally is from 1mW to 10mW, the voltage on a resistive load only changes by a factor of  $\sqrt{10}$ . This is consistent with the approximation made in Chapter 4 that treated the internal load as a resistor.

Figure 5-5 shows the conceptual diagram for the feedforward controller. The

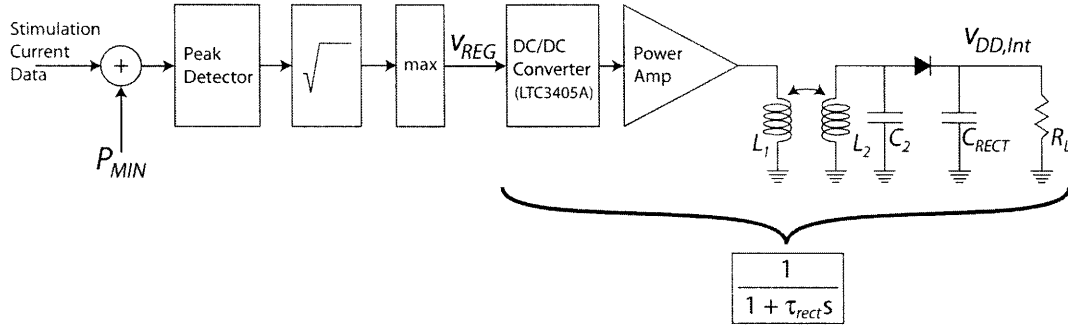


Figure 5-5: Block diagram of feedforward control for just-needed power.

current data stream is peak detected with a current-mode asymmetric time-constant filter similar to the one used in the AGC to extract the maximum current. It is also possible that during periods of silence the data stream indicate the need for zero stimulation power. A practical implanted unit could still require a small amount of static power; therefore, a minimum power level should also be available. A DC current, representing a minimum power level, is added to ensure the implanted unit has some power at all times. A subthreshold square-root circuit scales the currents and a maximum-current circuit ensures the power level does not exceed safety limits.

In Figure 5-5 the time constant due to the power system is small compared to the rate of change of speech signals. The dynamics of the charging and discharging of the implanted supply voltage are dominated by the effect of the rectifier charging the capacitor,  $C_{RECT}$  and the rectifier resistance. I have modeled these dynamics with a first-order time-constant,  $\tau_{rect}$ . This time-constant can be computed from nonlinear simulations; however, I have measured this time-constant under our operating condition and found it to be quite fast.

The effective time constant for the entire power system using the design described in Chapter 4 was  $\tau_{rect} \simeq 140\mu s$ . A large step in the required current could potentially appear before  $V_{DD,int}$  had time to charge. This issue could be addressed by introducing a small finite delay of several milliseconds in the stimulation currents to allow the implanted unit supply to charge. A patient's ability to use other sensory queues, such as lip reading, are not affected by delays of less than  $10ms$ . A potential stimulation



delay of  $4\tau_{rect}$  would, therefore, not be perceptually significant and should not affect patient performance.

### 5.2.2 Feedforward Controller Circuits

The digital CIS stimulation data is a parallel stream of seven bits. The low-power circuits to process this data stream and program the implant power are shown in Figure 5-6. Positive going transitions in an additional digital signal, the CIS clock, indicate when the data is valid to be latched. A set of edge-triggered latches store the bits and set the switch voltages for a current-mode digital to analog converter (DAC). To reduce overhead, I only use 16 power levels, therefore, only the four most significant bits  $D_7 - D_4$  are latched. The DAC circuit scales the reference current  $I_{DAC,Ref}$  by the four bit code with devices,  $M_1 - M_4$ . A DC current in  $M_5$  is added to set a minimum power level. The current reference was  $I_{DAC,Ref} = 10nA$  to ensure the subsequent translinear circuits would operate below threshold.

The peak detector circuit, consisting of devices  $M_6 - M_{10}$ , filters the DAC current with asymmetric time constants. This circuit is described in detail in [34]. The pair of devices  $M_7$  and  $M_8$  alternate which capacitor is charged,  $C_a$  or  $C_r$ . This results in one time constant  $\tau_a$  for increasing currents and another time constant  $\tau_r$  for decreasing current. I chose the time constants such that the charging time would be short in comparison with stimulation rate, i.e.  $\tau_a \simeq 200ns$ . A release time constant that is relatively slower than the attack time constant gives this circuit a peak detection effect. Choosing a release time constant that is roughly the length of a frame CIS data ( $\tau_r \simeq 2ms$ ) assures that the highest power level needed during the frame is transmitted to the implant.

A square-root circuit then maps the 16 current levels to a scale that will correspond to a change in power level of a factor of 10. Computing the translinear circuit operation by summing the gate-source voltages of devices  $M_{11} - M_{14}$ , and equating the product of the currents, I obtain,

$$i_{PROG}^2 = i_{FILT} I_{SQRT}. \quad (5.6)$$

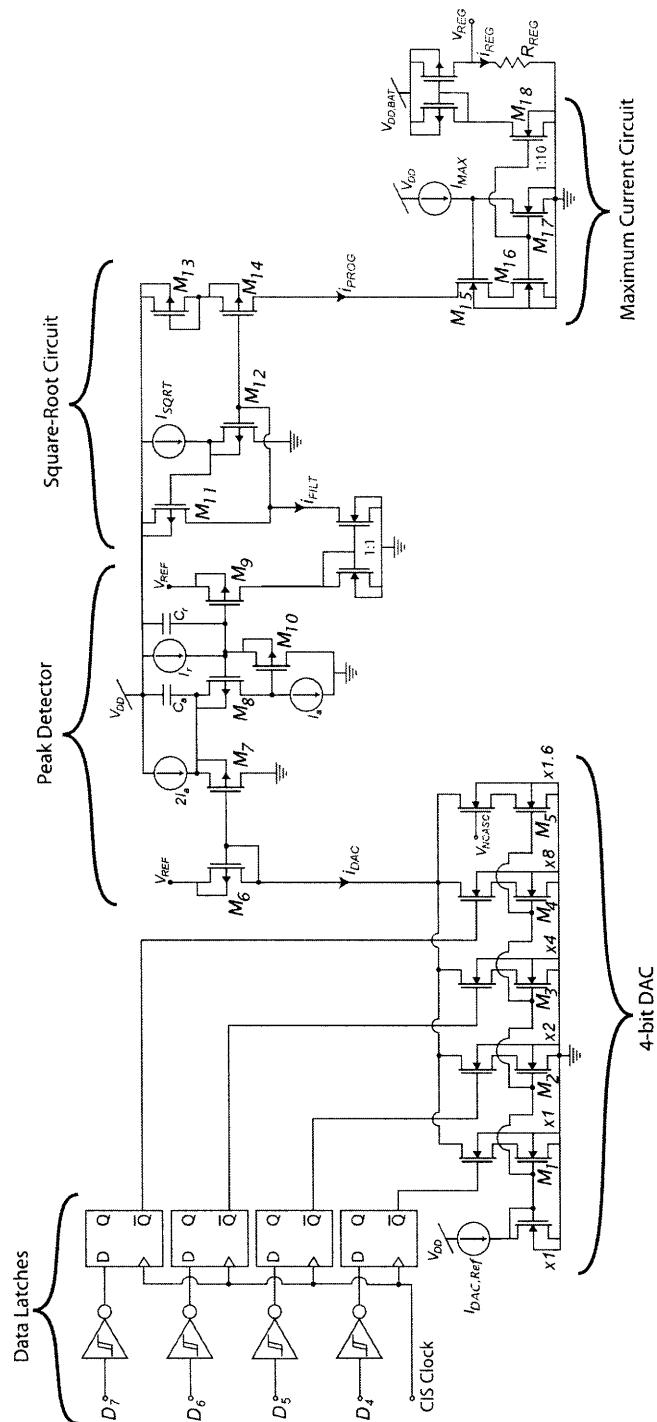


Figure 5-6: Feedforward circuits control the power level dynamically. Circuits are described in the text.

Finally, the program current  $i_{PROG}$  is compared with a maximum current,  $I_{MAX}$ . To protect the implant from operating above a maximum power level, the smaller of these two currents conducts to the output. A scaling factor of 10 reduces the size of the resistor needed at  $R_{REG}$  which ensures that parasitic capacitance at the  $V_{REG}$  node will not slow down the controller response.

### 5.3 Results

The low-power cochlear implant system was assembled on a PCB board, shown in Figure 5-7, to test the functionality of the power system. While the board that demonstrates this functionality is large ( $4'' \times 7''$ ), miniaturization of this system is not difficult. Most of the critical off-chip components are done with surface mount versions to ensure that the efficiency can still be achieved with a small physical footprint. The chips were mounted in standard ceramic test packages. To reduce their footprint these ICs can be mounted directly with chip-on-board techniques to drastically reduce the area.

A 2.8-V supply provides power to the ABEP chip and the analog components on the power system chip. A 1.8-V supply powers clock generation and digital controller on the power system chip. The CIS data stream and clocking information is streamed from the bionic ear chip to the power system chip. Audio inputs were done using an auxiliary connection as well as the FG-3329 microphone.

The cochlear implant board was tested for two sets of conditions. First, the system was tested to demonstrate the data dependent power level programming using the switching regulator. I also tested this system without the regulator to show how the system would perform at a static power level and without the inefficiency of the regulator.

In both of these tests the stimulation load was modeled with a passive resistor  $R_L$ . This simplified arrangement allows me to test the efficiency without implementing a particular stimulation scheme. I have shown above that using a passive load is a reasonable approximation to the CIS stimulation strategy.

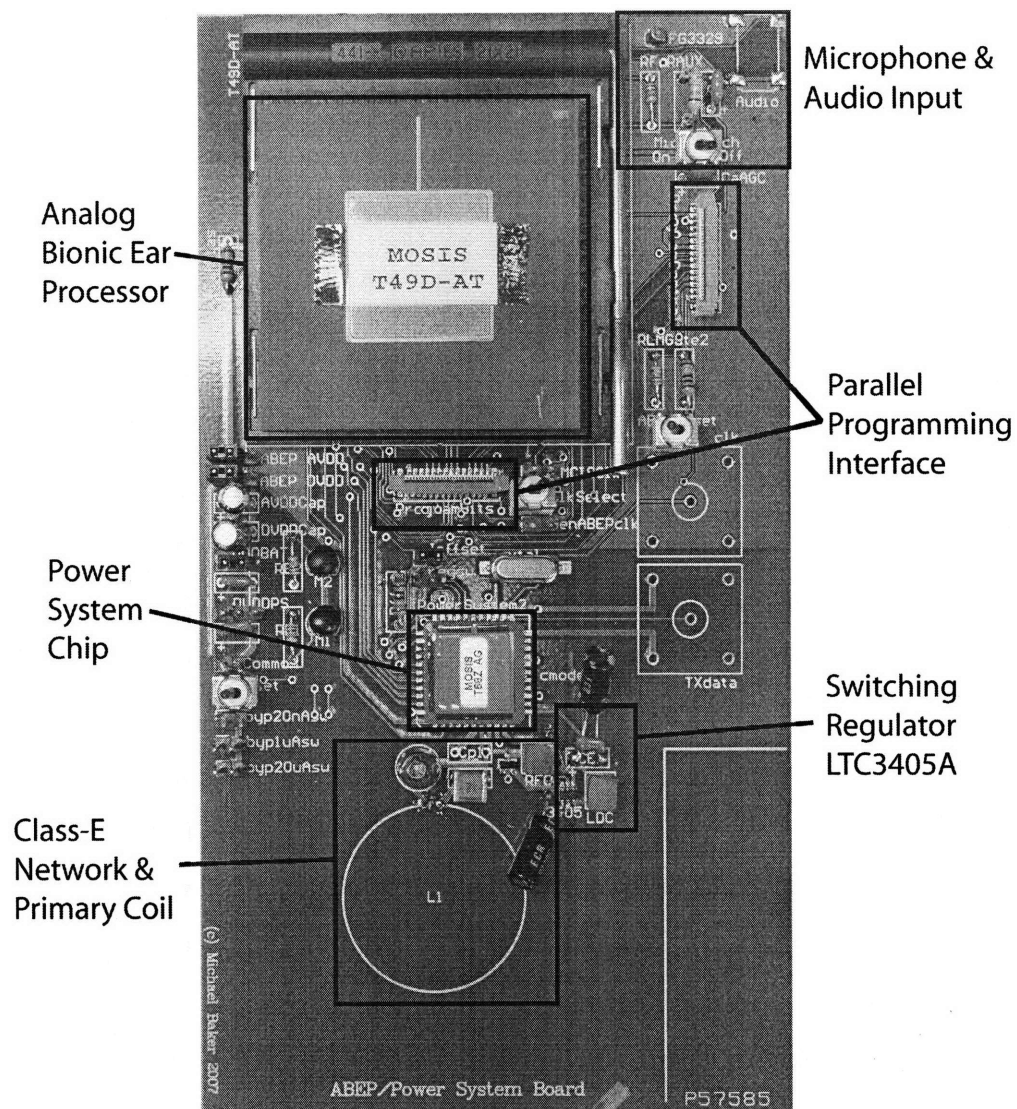


Figure 5-7: A photo of my implant system test board shows the analog bionic ear processor (ABEP) and the power system chip. A programming interface allows configuration of 86 patient parameters. The secondary board with the rectifier and resistive load model are not shown.

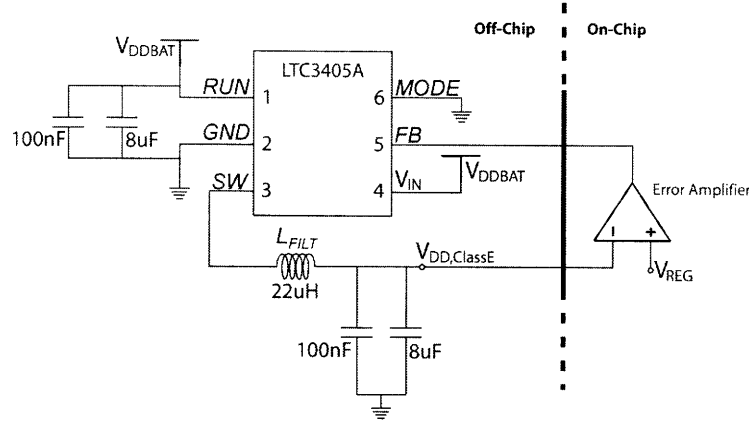


Figure 5-8: The off-the-shelf switching regulator configuration is shown with the output network and feedback control from the power chip. The battery and output supply voltages were bypassed with ceramic and electrolytic capacitors to improve ripple rejection and stability.

### 5.3.1 Feedforward Control Performance

The range of  $V_{REG}$  was set by an off-chip pull-down resistor,  $R_{REG}$ , of  $2M\Omega$ . Both  $I_{SQRT}$  and  $I_{MAX}$  were set on-chip to  $85nA$  and  $120nA$ , respectively. The peak output current was  $1.2\mu A$  for a maximum control voltage of  $2.4V$ . A set of power system chips were tested and the maximum output current varied by 12% over three tested chips. The power regulator was configured as shown in Figure 5-8 with feedback control of the output voltage from the power system chip.

Figure 5-9 shows a sweep of the digital code control from the ABEP under these conditions. The roughly square-root relationship of input current to regulator voltage produce an almost linear relationship in the power dissipated in the resistive load.

Figure 5-10 shows a breakdown of the power dissipation for the various components of the implant system. The quiescent power, including the clock generator circuits, the signal processing in the ABEP, and the power system control circuits, were measured once and assumed constant for all coil separations. These constant dissipations from both the  $2.8V$  and  $1.8V$  supplies total  $498\mu W$ . The **Useful Power** line represents the sum of power used to process the signal and the power delivered to the implanted load. The measured points, indicating the **Total Power Consumption**, indicate all

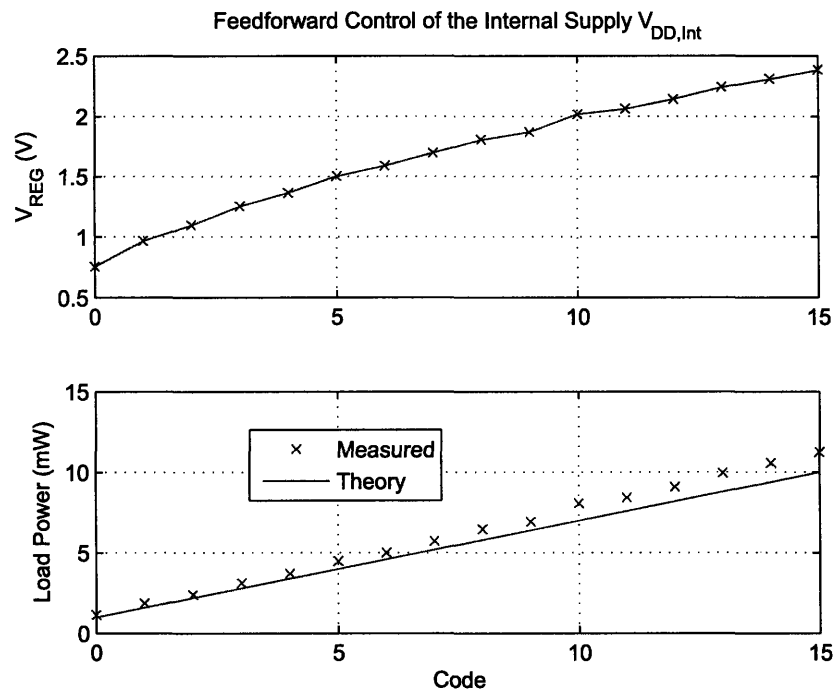


Figure 5-9: A sweep of the power level is shown for the 16 possible input codes. The top trace shows the regulator voltage,  $V_{REG}$ . The bottom trace shows the power dissipated in the internal stimulator for all code settings.

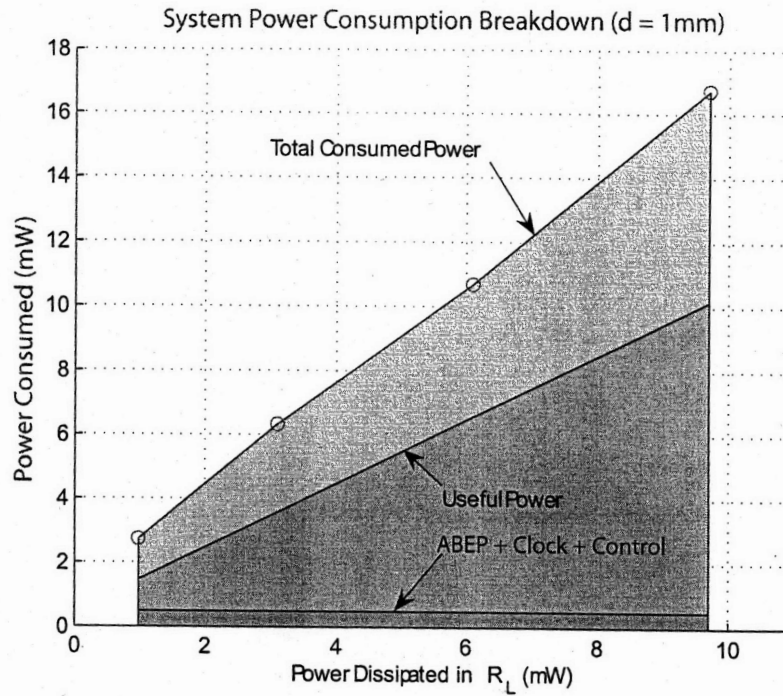


Figure 5-10: A breakdown of the power consumption in the implant board is shown for a feedforward power control case at 1mm coil separation. Constant power dissipations; ABEP, clock generator, and control circuits, were measured and assumed to be constant for all operating power levels. The **Useful Power** represents the total power delivered to the load,  $R_L$ , plus the constant power dissipation terms.

of the power consumption from both supplies. Table 5.4 summarizes the results for 1mW load power at several coil separation distances.

### 5.3.2 Fixed Power Performance

The feedforward system relies on the LTC3405 switching converter to set the Class-E supply voltage. Unfortunately, this converter has a great deal of power overhead and

Table 5.4: Total Power Consumption for 1mW Load Power of Feedforward Control Bionic Ear System

Coil Separation Distance, $d$ (mm)	Total Power (mW)
1mm	2.86mW
6mm	3.01mW
10mm	3.5mW

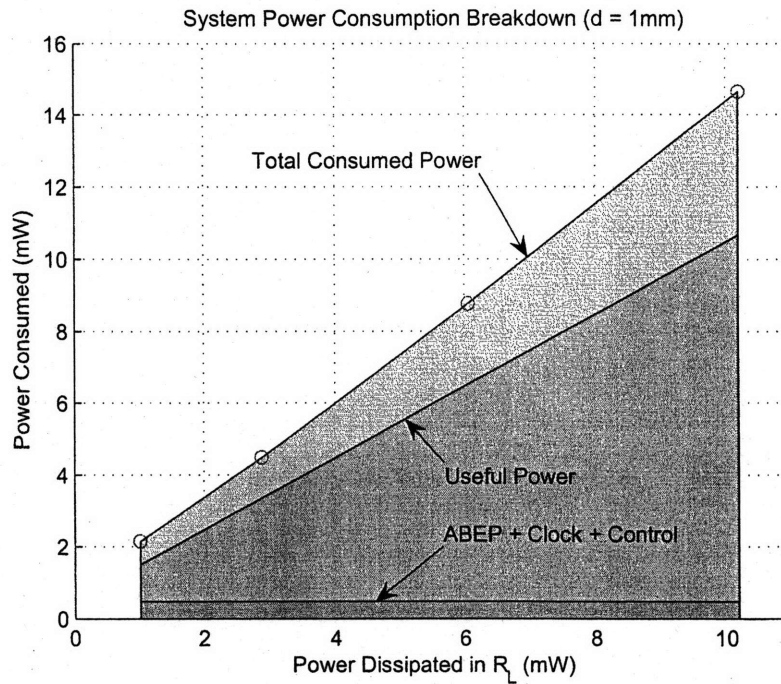


Figure 5-11: A breakdown of the power consumption in the implant board is shown for a fixed power level case at 1mm coil separation. Constant power dissipations; ABEP, clock generator, and control circuits, were measured and assumed to be constant for all operating power levels. The **Useful Power** represents the total power delivered to the load,  $R_L$ , plus the constant power dissipation terms.

is ill-suited for low-power loads, i.e. below 10mW. A set of performance metrics for a fixed Class-E supply voltage, generated ideally in the lab, shows more clearly the performance of the circuits designed in this thesis. Note that a more suitable power amplifier design, one in which the transmitted power level could be modulated more simply, is desirable. Appendix C discusses just such a design.

Figure 5-11 shows a breakdown of the power dissipation for this fixed power configuration. In this case, the measured points indicating the **Total Power Consumption**, indicate all of the power consumption from both 1.8V and 2.8V supplies as well as a third supply for the Class-E voltage. Table 5.5 summarizes the total power consumption for a 1mW load power at several coil separation distances.



Table 5.5: Total Power Consumption for 1mW Load Power of Fixed Power Bionic Ear System

Coil Separation Distance, $d$ (mm)	Total Power (mW)
1mm	2.21mW
6mm	2.36mW
10mm	2.76mW

## 5.4 Summary

Using the systems described in Chapters 2, 3, and 4, and a low-power bionic ear processor, I have demonstrated a low-power cochlear implant signal and power processing system. My design implements an adaptive power transmission scheme to provide the needed power at the implanted unit and minimize the wasted power in the stimulator circuits for power levels from 1mW – 10mW.

At a load power consumption of 1mW and coil separation of 6mm, I measured 3mW of total power consumption from the 2.8V and 1.8V supplies. If I remove the switching regulator losses and fix the delivered power level, the power drops to 2.36mW. This demonstrates a low-power 80dB-input high-PSRR system with better than  $10\times$  improvement from traditional cochlear implant designs.

This power is the lowest reported for a system that includes a wide dynamic range programmable front-end, cochlear implant channel processing, a transcutaneous power system and power consumption of the electrode array. This low power level means lower cost implant systems as well as better reliability and autonomy for cochlear implant patients.

## 5.5 Lessons of this Thesis

Each of the systems I have explored in this thesis represents a set of lessons on low-power mixed signal systems design. To build a low-power cochlear implant has required innovation in three areas. First is the design of low-power, flexible, and noise-immune front ends. Second, intelligent management of dynamic range has been accomplished by hybrid control of a feedback gain control circuit. Finally, a low-

power transcutaneous power link that uses a feedback method for optimized efficiency performance has been demonstrated.

### 5.5.1 Low-Power Analog Front End

The front end was designed around a sense-amplifier topology. This design gave me the flexibility to multiplex auxiliary input signals, each with its own gain settings. Using feedback to remove DC current from the microphone signal improves the signal swing and reduces the power consumption of the output stage. Moreover, using feedback to regulate the microphone circuit helped to reduce noise coupling from the supply.

The integrated supply filters were critical to realizing supply immunity in the noisy environment of a mixed-signal bionic ear system. Like traditional supply filters that attempt to trade output voltage swing for supply immunity with passive filters, my system sacrifices some output range. Because my design is active, however, I am able to take advantage of the high output impedance of MOS devices to attenuate supply noise coupling. A brief comparison of passive supply filters and active supply filters is given in Appendix A.

### 5.5.2 Dual-loop AGC

In the dual-loop AGC, I am trying to build a system which adapts to both short-term information in the signal as well as long-term trends in the signal. My signal processing strategy in the dual-loop AGC system used low-power decision circuits and implicit state storage to avoid digitization of the wide dynamic range signals. Each decision about a transition between fast control and slow control represents a decision about the information in the sound waveform.

A conventional signal processing approach would proceed by digitizing the analog signal as soon as possible. This is a more general solution because then the cost of making *any and all* decisions concerning the signal state are already precomputed. That is to say that quantization, as performed by an analog-to-digital converter,

is a form of deciding what the value of the signal is at all times within some bit precision and sample timing. As a result, signal processing using the conventional signal processing strategy is more power intensive requiring a digitally programmable variable gain amplifier, high-speed A/D converter and a DSP [5].

In this sense, both the dual-loop AGC system and the ABEP system share a common economy: By delaying digitization until the information has been processed into a convenient and information-dense (i.e. low-bandwidth and low-SNR) form, hybrid analog computation avoids unnecessary discrete computations [7].

The challenge for analog computation continues to be whether the robustness and programmability of digital systems can be retained in a low-power analog implementation of a comparable algorithm. My AGC demonstrates programmability of six compression parameters and can implement an intelligent speech compression algorithm with significantly less power consumption than A/D-DSP based designs.

### 5.5.3 Transcutaneous Inductive Power Links

In this thesis, making an efficient power link required focus on two areas. First, a feedback model of the losses in magnetically coupled resonators yielded a maximum efficiency design for the secondary circuit. Second, a simple low-loss power driver was designed around the principle of minimizing switching losses.

The feedback model yielded the insight that a tradeoff exists between the energy distribution in the secondary coil and the efficiency of energy coupling between the primary and the secondary. I provide a closed form solution for the optimal loading condition and outline a design procedure for the primary and secondary circuit parameters. By choosing a Class-E power amplifier topology that minimizes switching losses the efficiency of these two blocks together is asymptotic to the predicted theory.

The problem with this approach is that it did not simultaneously consider the energy wasted in controlling the power level of this amplifier continuously. The only convenient way to change the power level in this amplifier is to change the supply voltage. Instead, a more comprehensive power amplifier would have been able to easily change the power level, while still achieving a reasonably high power efficiency.

A Class-D driver design, discussed briefly in Appendix C, would have been a better choice for overall system integration with power control.

#### **5.5.4 Transcutaneous Bionic Ear System**

I have built a board that puts the systems described in this thesis together. The performance of this board shows the promise of the low-power processing techniques for a cochlear implant discussed in this thesis. The key ideas that have made this possible are my low-power analog signal processing strategy, a feedback model for efficient magnetic power transfer, and low-loss power driver. The motivations that initiated this thesis work were to lower the cost of implanted hearing instruments to make them a viable choice for more people in the world. If these techniques can be applied in future designs then this effort has been well worth the time and sacrifice that it required.

# Appendix A

## Comparison of Passive and Active Supply Filters

In Chapter 2, I presented a cascoded DC current source design that filters the supply voltage to prevent in-band noise from coupling into the active analog circuits. This appendix clarifies the benefits of this approach over output filters or passive supply filters.

To filter noise from the supply, there are several systems approaches. One strategy is to include filters in the output of the sense amplifier, subsequent to the amplifier altogether. Another strategy is to filter the supply directly, before it gets to sensitive signal processing circuitry. To maximize the attenuation of unwanted signals prior to A/D and nonlinear stages, which can rectify unwanted noise and produce aliasing, all of these strategies can be used together.

Consider the active elements in the filters presented in Chapter 2. These devices could have been replaced with resistors. Using an active device as the filter element, however, has the advantage of high saturation output resistance without the voltage drop associated with a passive resistance of the same size. This has the added benefit of reducing the low-pass filter rolloff corner. The power consumption and roll-off frequency of series supply filters are summarized in Table A. For these results, I have assumed a DC current of  $I_{DC}$  flowing through the elements, as well as a filter capacitor,  $C_{FILT}$ .

Table A.1: Some Figures of Merit for Active and Passive R-C Supply Filters

	R-C Lowpass	Active: Above $V_T$	Active: Below $V_T$
Power Dissipation	$I_{DC}^2 R_{FILT}$	$\geq I_{DC} \kappa (V_{GS} - V_T)$	$\geq I_{DC} 6\phi_t$
Rolloff Frequency	$\frac{1}{R_{FILT} C_{FILT}}$	$\frac{g_m}{C_{FILT}} \left( \frac{G_{GD}}{C_{GS} + C_{GD}} \right)$	$\frac{\kappa I_{DC}}{\phi_t C_{FILT}} \left( \frac{G_{GD}}{C_{GS} + C_{GD}} \right)$

## Appendix B

# Optimal Sizing of the Power Switch in the Class-E Power Amplifier

In Chapter 4 I described a simple but efficient power driver for transcutaneous implants. I presented an overall efficiency analysis that emphasized the quality factor of the resonators. This appendix explores the Class-E driver efficiency by attempting to account for conduction and switching losses in each of the components. I will also briefly describe how to choose the device sizing to minimize conduction and switching losses at the same time.

The amplifier of interest is shown in Figure 4-10. The active device to be optimized,  $M$ , acts as a switch to alternate between open and short circuit to ground at the node  $v_d$ . Losses in the DC/AC converter due to this switch are critical to efficiency because current in the inductor,  $L_{RFC}$ , conducts through this device. Also, the device provides a path through which the  $L_1$ - $C_1$  network resonates.

### B.1 nMOS Switching Device

Each power switch device was composed of many parallel devices each  $12\mu m$  wide by  $0.5\mu m$  long in the AMI MOSIS  $0.5\mu m$  CMOS process. Each device has a measured gate capacitance of approximately  $21fF$ . With  $V_{GS} = 1.8V$  the series resistance of this tiny device is roughly  $500\Omega$ . To scale the device for convenient integration and

IC layout, a multiplicity  $M$  of these unit devices are connected in parallel.

The series resistance of the switch devices can also be altered by changing the switching supply voltage. The limitation on this is that the other digital control circuits have less reliable startup below 1.6V. This is because the process threshold voltages are  $V_{Tn} \simeq 0.6V$  and  $V_{Tp} \simeq 0.9V$  for n- and p-devices, respectively. By reducing the digital supply voltage, I can save gate switching power, however, the clock generator startup is not as robust.

## B.2 Losses in Primary Circuit

Looking at the models for the Class-E circuit in both the FET-on and FET-off phases in Figure B-1. First, I assume that the primary resonator elements, including the feedback effect from the secondary, form a high-Q oscillator. This oscillator has an *rms* current of  $i_{rms}$  at all times during the switching cycle. I can write all of the power dissipation in the primary resonator during the FET-on phase,

$$P = |i_{rms}|^2 (R_{DS,on} + Z_1(1 - L(s))) \quad (B.1)$$

$$= \underbrace{|i_{rms}|^2 R_{DS,on} + |i_{rms}|^2 R_1}_{\text{Primary Conduction Losses}} + \underbrace{|i_{rms}|^2 \frac{\omega^2 M^2}{R_2'}}_{\text{Delivered to Secondary}}. \quad (B.2)$$

Using Eq. B.1, and knowing the power delivered to the secondary circuit, I can compute the other losses from device and element parameters. Some additional considerations need to be made to include approximate losses from the other elements in the Class-E amplifier.

### B.2.1 Switching Considerations

In hard switched amplifier topologies, like the one presented in this thesis, switch state changes will contribute to wasted charge. The class-E output network is intended to shape the drain transient waveform to ensure that no excess charge is present at the drain at the time when the FET device is switched on. For this reason, I will assume



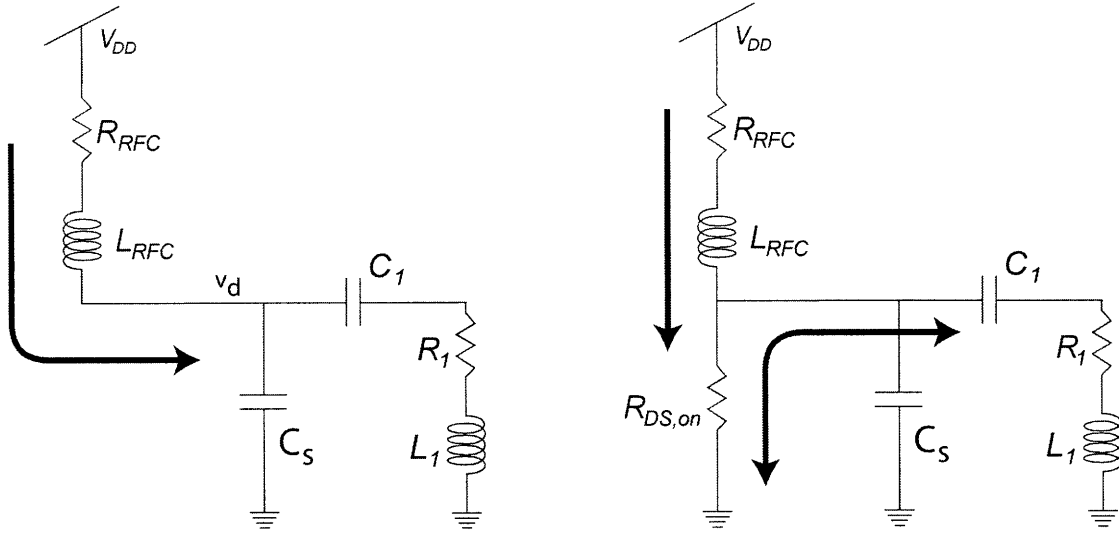


Figure B-1: The conditional linear circuits for a class-E amplifier are shown. On the left, the FET-off condition is shown with current from the radio frequency choke (RFC) charges the output network. On the right, the FET-on condition is shown. In this condition the output capacitance  $C_S$  is shorted to ground, the tank self-resonates and the RFC is fluxed by connecting it to ground.

for the analysis in this section that the charge wasted at the drain node is not a significant contributor to overall wasted power. Charge is wasted, however, at the gate node where an inverter is used to hard switch the node from  $0V$  to  $V_{DD}$  and back.

Unlike the linear resonator case above, the switching Class-E driver is a time-varying circuit. Several assumptions need to be made and discussed to continue with the analysis. The assumptions I am making are:

- The primary resonator is high-Q: When loaded by the secondary, the quality factor of the primary is roughly equal to the loaded quality factor of the secondary,  $Q'_1 \simeq Q_L$ . For my system, this quality factor is  $\sim 10$ . This value of this assumption is that current in the resonator can be approximated as a sinusoid.
- Duty Cycle of 50%: This is a useful assumption to avoid integrating over fractions of the cycle. Figure 4-14 shows that this is not altogether unreasonable.
- $I_{RFC} = |i_{rms}|$ : This assumes that the converter acts as a DC/AC current con-

verter. This is only strictly true if the converter is perfectly efficient. This assumption is, therefore, only useful as a lower bound for conduction losses in the choke inductor  $L_{RFC}$ .

- Soft switching of  $v_d$ : Because the output capacitance,  $C_s$ , is small, and the waveform shaping strategy for soft switching is at least partly effective over all coil separations, this is a reasonable assumption and greatly simplifies wasted power calculations.

In the FET-off case, the DC current in the choke is charging the drain node,  $v_d$ . If the duty cycle is approximately 50% I will approximate the average current in the radio-frequency choke (RFC) is also  $i_{rms}$ . Second, during the FET-on phase, this current is also conducted through the active device, contributing to conduction losses. I can also include the switching charge to drive the gate of the FET device at frequency,  $\omega/2\pi$ , from 0V to rail voltage  $V_{DD}$ . A new version of Eq. B.1 would be,

$$P \simeq \underbrace{|i_{rms}|^2 (R_{RFC} + 2.5R_{DS,on} + R_1) + fC_{gate}V_{DD}^2}_{\text{Wasted}} + \underbrace{|i_{rms}|^2 \frac{\omega^2 M^2}{R'_2}}_{\text{Useful}}. \quad (\text{B.3})$$

This form is only an approximate form for the losses in the Class-E driver, however, it is worth noticing a few effects. First, when the primary and secondary coils are very close together, i.e. the skin flap is thin, the “Useful” term will draw less current in the primary. This results in lower conduction losses and a higher proportion of switching losses. When the coils are well separated, however, conduction losses will become more significant.

To compute an effective efficiency of the Class-E and primary-secondary coupling given these approximate device losses, I write the ratio of useful to total power dissipations,

$$\eta \simeq \frac{|i_{rms}|^2 \frac{\omega^2 M^2}{R'_2}}{|i_{rms}|^2 (R_{RFC} + 2.5R_{DS,on} + R_1) + fC_{gate}V_{DD}^2 + |i_{rms}|^2 \frac{\omega^2 M^2}{R'_2}}. \quad (\text{B.4})$$

Using this form, and a breakdown of the different mechanisms, I can show the optimal

device sizing in the  $0.5\mu\text{m}$  CMOS technology. To compare with Figure 4-17, the efficiency metric being discussed in this appendix includes the controller efficiency, and primary-secondary coupling, but does not include the rectifier inefficiency, or the secondary efficiency.

### B.3 Design Performance

The design presented in Chapter 4 used a device with 100 of the fingered devices described above. Using Eqs. B.3 and B.4 I can compare the loss mechanisms given a delivered power level of 1mW, and various coil coupling factors corresponding to the varying skin-flap thicknesses that are encountered in patients.

The upper set of traces in Figure B-2 show the breakdown of all loss mechanisms in the primary class-E amplifier from Chapter 4. Notice that in this low-power situation, the conduction loss in the active devices are significantly greater than the gate switching loss. This indicates that a larger device, one with a lower series resistance, would produce better overall efficiency.

### B.4 Sizing the Device for Optimal Performance

If I now vary the multiplicity of the devices to achieve better performance over a variety of operating conditions. Figure B-3 shows a computation of the efficiency from Eq. B.4. The peak efficiency is seen shifting to a higher multiplicity as the coupling between the coils decreases. This can be explained by thinking about how the secondary impedance is reflected in the primary circuit changing the primary current.

At higher coupling the feedback impedance from the secondary is large, and only a small amount of current is needed to deliver the desired power to the secondary. Switching losses, therefore, are more critical at high coupling. Thus, for the  $k = 0.16$  case (near 1mm coil separation), the optimal device size is near  $M = 100$ , as fabricated. As the coils are separated, however, more current flows in the primary

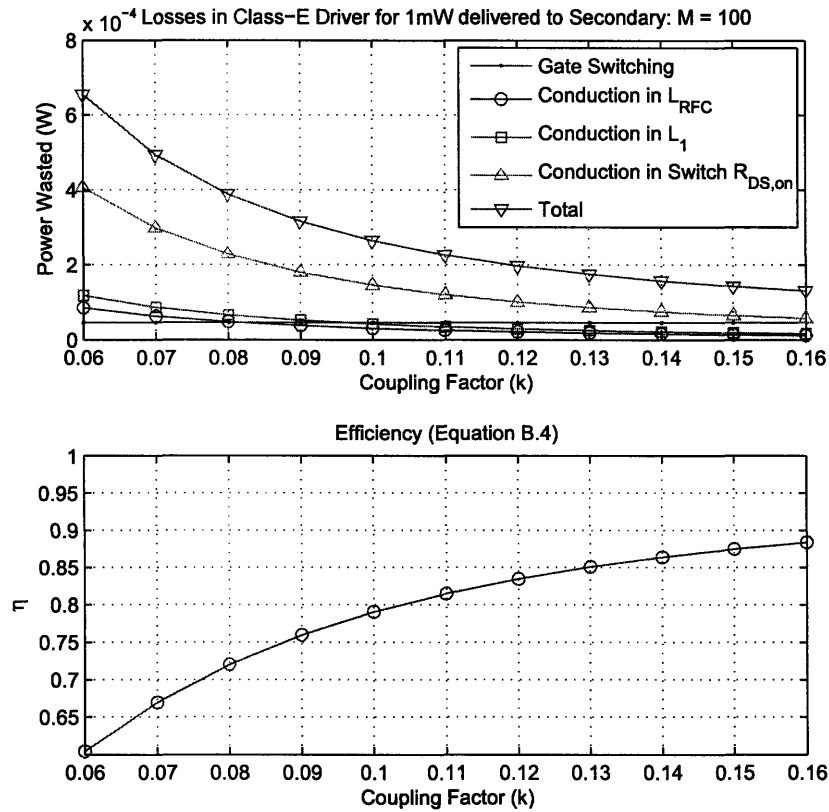


Figure B-2: The top set of traces show a breakdown of conduction and switching losses in the Class-E amplifier for a useful power of 1mW. The conduction loss in the switch dominates the losses in the system for the  $M = 100$  device. The bottom graph shows the efficiency from Eq. B.4 for a 1mW load power.

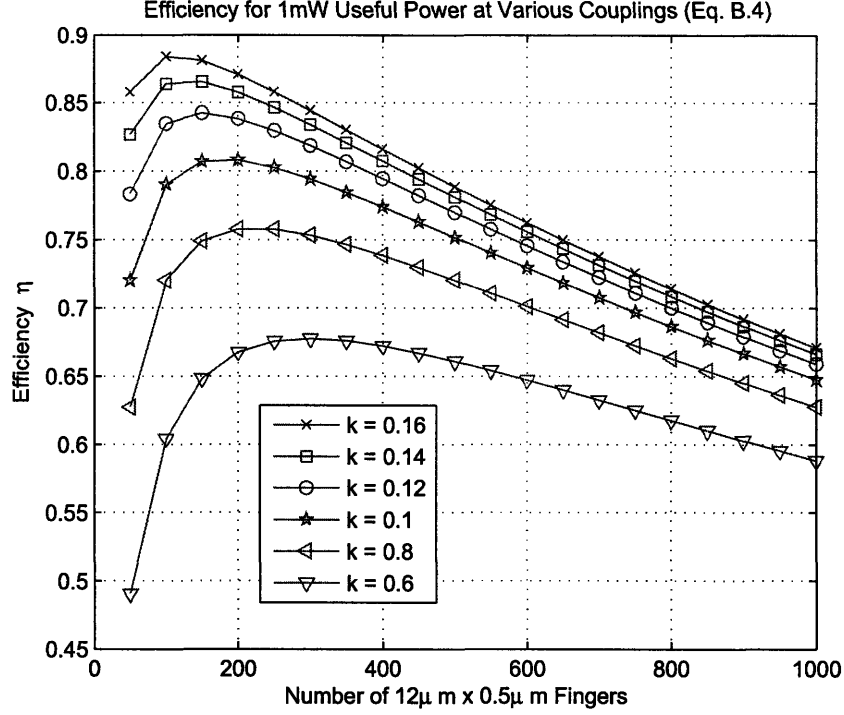


Figure B-3: A set of efficiency traces are shown for various coupling conditions. The optimal device sizing is different depending on coil separation due to changing current levels in the primary circuit.

circuit because feedback from the secondary circuit is weaker. In this case, larger devices are desirable because they produce less conduction loss.

Since a single size must be chosen for IC fabrication, a typical coupling could be chosen corresponding to an average skin thickness of 6mm, or  $k \simeq 0.1$ . From Figure B-3 multiplicity should be  $M \simeq 200$ . This ensures a good tradeoff between efficiency for thin skin and thick skin. A device with  $M = 200$  would have an  $R_{DS,on} \simeq 2.5\Omega$  and a gate capacitance of  $C_{gate} \simeq 4.2pF$ .

Choosing this new sizing, I can recompute the losses for various couplings or skin flap thicknesses. Figure B-5 shows the loss breakdown for the  $M = 200$  device and for 1mW load power. Notice that the switching power now dominates the losses for couplings above  $k \simeq 0.1$ .

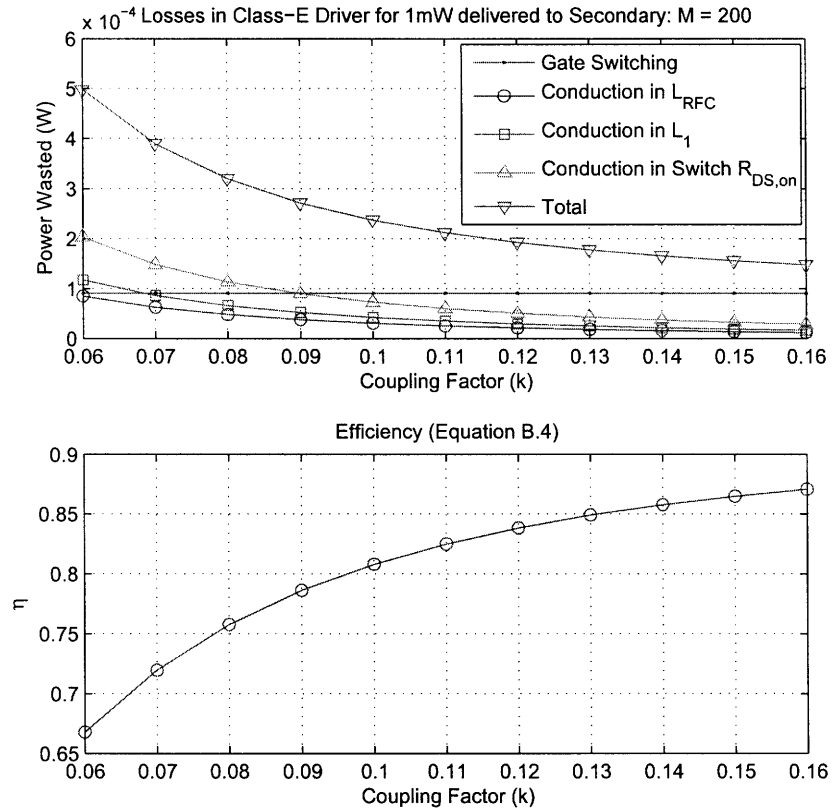


Figure B-4: A breakdown of conduction and switching losses in the Class-E amplifier for a useful power of 1mW. The conduction loss in the switch dominates the losses in the system for the  $M = 200$  device. The bottom graph shows the efficiency from Eq. B.4 for a 1mW load power.

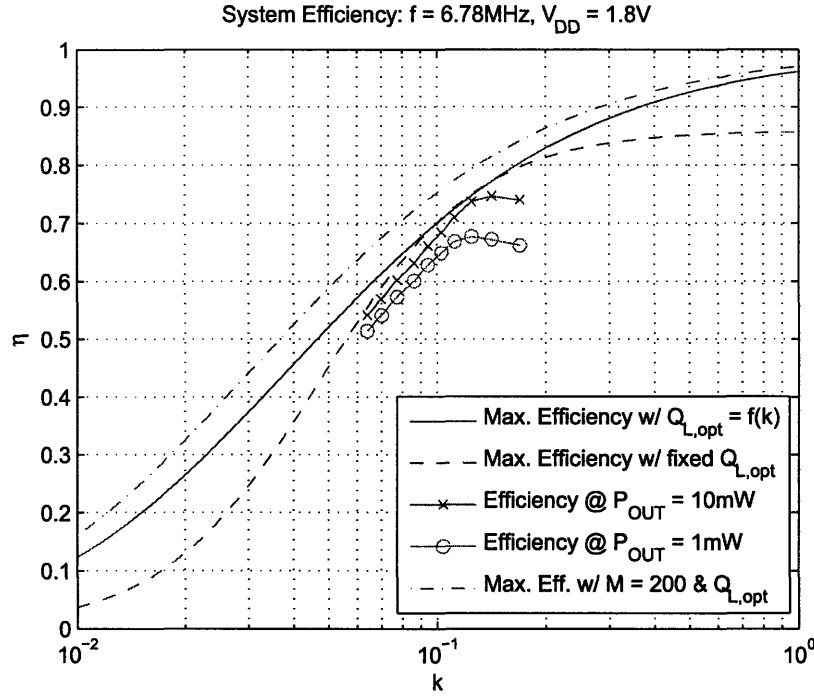


Figure B-5: The traces from Figure 4-16 are shown with an additional curve for the maximum possible efficiency given an improved primary quality factor,  $Q_1$ , from 35 to 51. The improvement in efficiency is anywhere from 4% to 7% over the range of couplings.

## B.5 Efficiency Comparison

In this appendix I have focused on an explicit computation of the losses, where in Chapter 4 I emphasized a quality factor based approach to computing efficiency. To reconcile these viewpoints I have computed how the effective  $Q$  of the primary would change for device multiplicities from  $M = 100$  to  $M = 200$ . The  $Q$  of the primary would improve from 35 to 51. This is a significant improvement considering the cost in gate drive power would only increase from  $46\mu W$  to  $95\mu W$  for  $1mW$  of useful power.

Figure B-5 shows a comparison trace with data from Chapter 4. In the coupling range of interest, an improvement of 4% to 7% can be realized by simply by choosing the device size more carefully.





## Appendix C

# Class-D Amplifier Design for Transcutaneous Power Links

The simplicity of the switching control in a Class-E topology is desirable because it reduces the amount of circuitry. Whatever benefit accrues from this, however, is lost because the power level of the Class-E system is not easily controlled. Indeed, in the system described in Chapter 5 over  $700\mu W$  of power are wasted in a poorly suited off-the-shelf switching buck converter.

A Class-D driver is another switching topology which could be better suited for driving the transcutaneous coupled resonators described in Chapter 4. It is better suited for two reasons. First, the voltage stresses on the integrated devices are reduced by hard switching them completely. Second, the power level can be controlled by changing the phase of the gate-drive signals [75]. This appendix describes the design and simulated performance of a Class-D amplifier.

### C.1 Class-D Power Amplifier

Figure C-1 shows a simple model of a bridged Class-D converter. Devices  $M_1$  and  $M_2$  switch like a digital inverter, alternately connecting the node  $v_{d1}$  to  $V_{DD}$  or ground. Devices  $M_3$  and  $M_4$  switch  $v_{d2}$  with the opposite phase to maximize the AC voltage across the resonator network,  $L_1 - C_1$ . To switch the stacked nMOS devices,  $M_1$

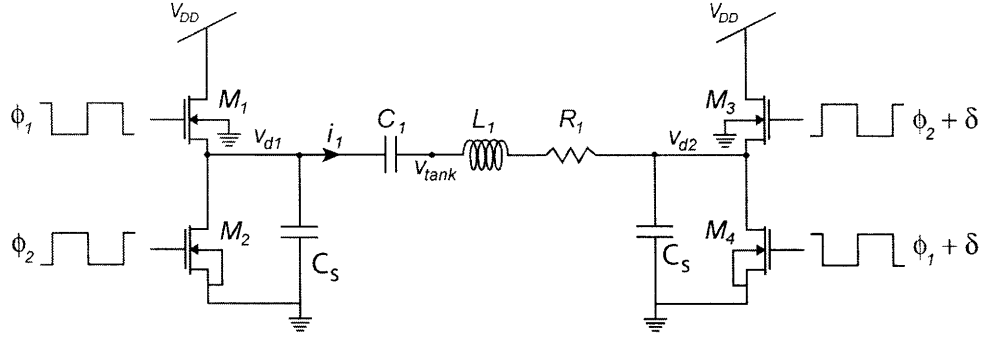


Figure C-1: A bridged Class-D topology is shown. Active devices hard-switch the drain nodes,  $v_{d1}$  and  $v_{d2}$ . Power level can be controlled by delaying the switching waveform by a phase angle,  $\delta$ .

and  $M_3$ , requires a gate-drive network which references the gate-drive signal to the sources,  $v_{d1}$  and  $v_{d2}$ . This can be accomplished with a transformer gate-drive [75], or with a dedicated supply rectified from the primary circuit using a diode-capacitor network [74].

To change the power level, the right-most device switching voltages can be shifted by some phase delay  $\delta$ . This has the effect of reducing the pulse width of the square wave across the resonator network, reducing the overall power level. This power-control strategy is more efficient because it does not require changing the supply voltage,  $V_{DD}$ , with a separate converter.

Unlike the Class-E there is no attempt made to soft-switch the drain capacitances,  $C_s$ . Also, there are more device gates to switch. Note that the additional losses of this design may seem counterproductive, however, this design affords the major benefit of simple control of the power level. As for generation of the device control waveforms, changing the phases of the gate-drive waveforms could be performed by a tapped delay line [76].

### C.1.1 Class-D Design and Optimization

The coupled magnetic resonators can be designed in the same way as the set in Chapter 4 as a similar design procedure is applicable. I will assume that the same quality factors can be achieved for elements in the primary and secondary circuits.

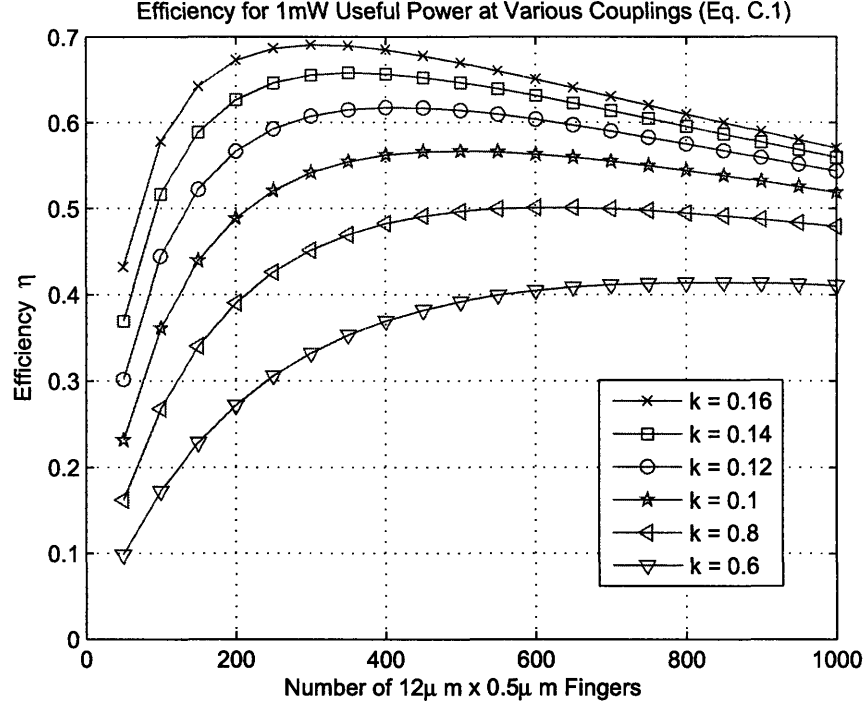


Figure C-2: The efficiency, computed from Equation C.1, is plotted for various device sizings. Losses in the rectifier were not included in this calculation.

I can compute the losses in this system in an approximate fashion by summing all of the power dissipations in the circuit using an approach similar to the one used in Appendix B for the Class-E amplifier. The series resonant circuit will conduct in phase with the switching waveform, therefore, the conduction loss of the active devices contributes in a similar way to the series resistance,  $R_1$ . Writing the total power in the circuit,

$$P = |i_{rms}|^2 \left( R_1 + 2R_{DS,on} + \frac{\omega^2 M^2}{R'_2} \right) + 4fC_{gate}V_{gate}^2 + 2fC_sV_{DD}^2. \quad (C.1)$$

Following a similar procedure to Appendix B, I can compute an optimal device size and plot the approximate efficiency for various switch sizings. Note that for this design, the switching losses are proportionally larger, therefore, I would expect that a smaller device size will be closer to the optimal efficiency condition.

Using Figures C-2 and C-3 I have chosen a multiplicity  $M = 500$  for the Class-D.

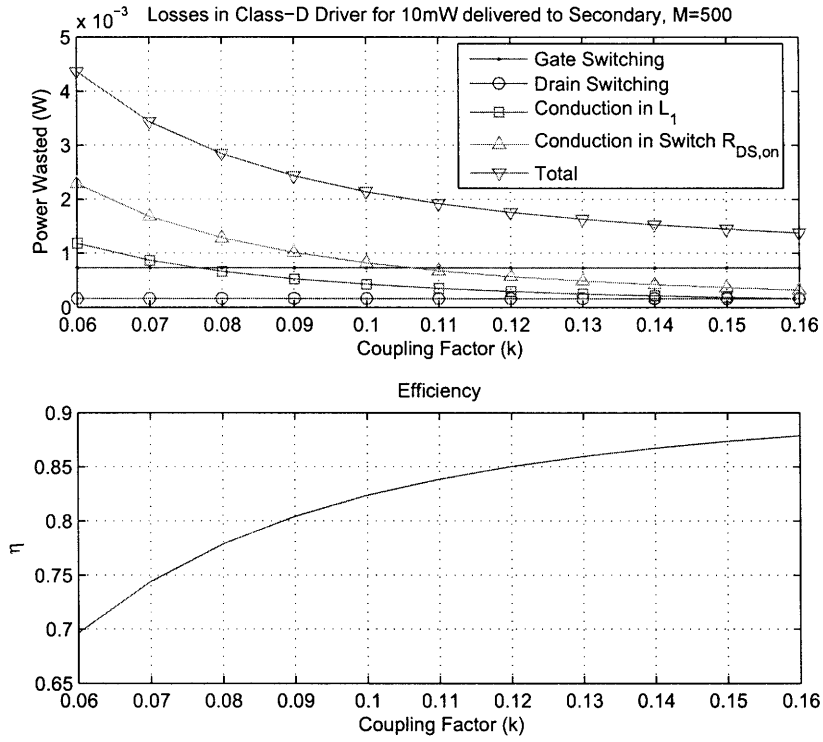


Figure C-3: A breakdown of the loss mechanisms is shown as the coil coupling is changed for 10mW of power delivered to the load. This calculation assumed that maximum power was being delivered, i.e.  $\delta = 0^\circ$ .

Table C.1: Class-D Power Driver Simulation Parameters

Parameter	Value
$L_2$	$6.42\mu H$ $Q_2 \simeq 90$
$C_2$	$77\text{pF}$
$L_1$	$5.5\mu H$ $Q_1 \simeq 90$
$C_1$	$100\text{pF}$
Switching Devices	$M = 500$ $12\mu m \times 0.5\mu m$
$V_{DD}$	$1.2\text{V}$
$V_{gate}$	$1.8\text{V}$
Rectifier Model	HBAT5400

This provides the best tradeoff between switching and conduction losses for average coupling factors. Note that these calculations were done for the maximum power level, where the switching waveforms for the right and left inverters are completely out of phase, i.e.  $\delta = 0^\circ$ . At higher  $\delta$ , where the power level is lower, the conduction occurs over a shorter fraction of the cycle, breaking the assumptions that make the simple Equation C.1 possible.

## C.2 Simulation Results

To simulate this alternative power amplifier topology, I chose the primary and secondary networks according to similar considerations from Section 4.2. In the secondary network, I included the Schottky rectifiers to model rectifier losses. I included the power consumption of a simple gate-driver circuit for calculation of the total power consumption. The parameters used for these simulations are summarized in Table C.1. The gate drive voltage swing  $V_{gate}$  is considerably larger than the power supply voltage  $V_{DD}$  to drive the devices well into triode conduction.

### C.2.1 Efficiency

Figure C-4 shows two sets of traces. First, the power level is shown varying with the conduction angle. An optimum coupling of  $k \simeq 0.1$  was chosen to obtain some power-level immunity to changes in coil separation. The efficiency is plotted below these traces for the same set of conduction angle conditions. Since these curves account for

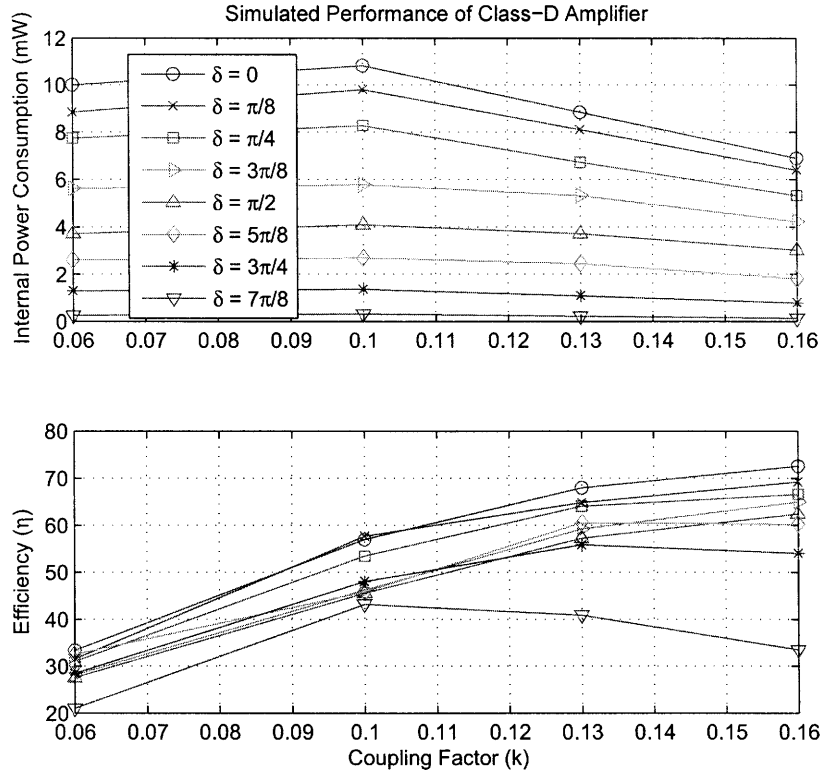


Figure C-4: Power level and efficiency are shown for various phase angles,  $\delta$ .

the rectifier losses, the efficiency is considerably lower at lower power levels.

To get a sense of how much benefit a Class-D power driver would have for the system presented in Chapter 5, consider the operation at an internal power level of 1mW and a coupling of  $k = 0.1$ , corresponding to approximately 6mm coil separation. Under these conditions, the total power consumption of the hypothetical Class-D system would be 2.5mW. This simulated design compares favorably with the feedforward design presented in Chapter 5 which consumes 3.01mW under the same conditions. Considering that a Class-D power driver places reduced voltage stress on the active devices, this would improve the robustness of a fully integrated design.

# Bibliography

- [1] National Center for Health Statistics, *Data from the National Health Interview Survey*, Series 10, No. 222, Table 11, 2002.
- [2] Loizou, P. C., "Introduction to Cochlear Implants," *IEEE Engineering in Medicine and Biology*, Vol. 18, No. 1, Jan. – Feb. 1999.
- [3] Dillon, H., "Hearing Aids," Thieme, 2001.
- [4] Moissl, U., Meyer-Base, U., "A comparisson of different methods to assess phase-locking in auditory neurons," *Engineering in Medicine and Biology Society*, Vol. 2, pp. 840-843, 2000.
- [5] George Gata, D., "A 1.1-V 270- $\mu$ A Mixed-Signal Hearing Aid Chip," *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 12, Dec. 2002.
- [6] Baker, M. W., Lu, T. K.-T., Salthouse, C. D., Sit, J.-J., Zhak, S., Sarpeshkar, R., "A 16-channel analog VLSI processor for bionic ears and speech-recognition front ends," *Proceedings of the IEEE 2003 Custom Integrated Circuits Conference*, pp. 521-6, Sept. 2003.
- [7] Sarpeshkar, R., "Analog Versus Digital: Extrapolating from Electronics to Neurobiology," *Neural Computation*, Vol. 10, no. 7, pp. 1601-38, Oct. 1998.
- [8] Moore, B. C. J., Glasberg, B. R., Stone, M. A., "A comparison of four methods of implementing automatic gain control (AGC) in hearing aids," *British Journal of Audiology*, Vol. 22, pp. 93-104, 1988.

- [9] Neuman, A. C., Bakke, M. H., Hellman, S., Levitt, H., "Effect of compression ratio on a slow-acting compression hearing aid: Paired-comparison judgements of quality," *Journal of the Acoustical Society of America*, Vol. 96, no. 3, Sept. 1994.
- [10] Victor, W. K., Brockman, M. H., "The application of linear servo theory to the design of AGC loops," *Proceedings of the IRE*, Vol. 48, pp. 234-8, Feb. 1960.
- [11] Ghovanloo, M., Najafi, K., "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," *IEEE Transactions on Circuits and Systems*, Vol. 51, No. 12, Dec. 2004.
- [12] Kendir, G. A., Liu, W., Wang, G., Sivaprakasam, M., Bashirullah, R., Humayun, M. S., Weiland, J. D., "An optimal design methodology for inductive power link with class-E amplifier," *IEEE Transactions on Circuits and Systems*, Vol. 52, No. 5, May. 2005.
- [13] Marsmar, E. D., Senger, R. M., Carichner, G. A., Kubba, S., McCorquodale, M. S., Brown, R. B., "A DSP architecture for cochlear implants," *IEEE International Symposium on Circuits and Systems*, pp. 82-6, May. 2006.
- [14] Kim, S., Lee, J.-Y., Song, S.-J., Cho, N., Yoo, H.-J., "An energy-efficient analog front-end circuit for a sub-1V digital hearing chip," *Symposium VLSI Circuits Digital Technology Papers*, pp. 176-179, Dec. 2005.
- [15] Cheng, A. K., Rubin, H. R., Powe, N. R., Mellon, N. K., Francis, H. W., Niparko, J. K., "Cost-Utility Analysis of the Cochlear Implant in Children," *Journal of the American Medical Association*, Vol. 284, No. 7, August 2000.
- [16] Moore, B. C. J., "Hearing loss in the elderly and its compensation with hearing aids," *Gerontechnology*, Vol. 1(3), pp. 140-152, March 2002.
- [17] Walden, R. H., "Analog-to-digital converter survey and analysis," *IEEE Journal of Solid State Circuits*, Vol. 17, no. 4, pp. 539-50, Apr. 1999.



- [18] Tang, Z., Sclabassi, R. J., Sun, C., Hackworth, S. A., Zhao, J., Cui, X. T., Sun, M., "Transcutaneous Battery Recharging by Volume Conduction and its Circuit Modeling," *Proceedings of the 28th IEEE Engineering in Medicine and Biology Society Annual International Conference*, New York City, pp. 644–7, Sept. 2006.
- [19] Lim, H. G., Yoon, Y. H., Lee, C. W., Park, I. W., Song, B. S., Cho, J. H., "Implementation of a Transcutaneous Charger for Fully Implantable Middle Ear Hearing Device," *Proceedings of the 27th IEEE Engineering in Medicine and Biology Society Annual International Conference*, Shanghai, pp. 6813–6, Sept. 2005.
- [20] Goto, K., Nakagawa, T., Nakamura, O., Kawata, S., "An Implantable Power Supply with an Optically Rechargeable Lithium Battery," *IEEE Transactions on Biomedical Engineering*, Vol. 48, No. 7, pp. 830–3, July 2001.
- [21] Hu, Y., Gervais, J.-F., Sawan, M., "High power efficiency inductive link with full-duplex data communication," *IEEE 9th International Conference on Electronics, Circuits and Systems*, Vol. 1, Sept. 2002.
- [22] Orneni, O., Toumazou, C., "A CMOS micropower wideband data/power transfer system for biomedical implants," *IEE Proceedings of the 2003 International Symposium on Circuits and Systems*, Vol. 5, May 2003.
- [23] Kuszta, B., "Silicon Cochlea," *Proceedings of the IEEE Wescon '98*, pp. 282–5, 1998.
- [24] Serdijn, W. A., van der Woerd, A. C., Davidse, J., van Roermund, H. M., "A low-voltage low-power fully-integratable front-end for hearing instruments," *IEEE Transactions on Circuits Systems I, Fundamental Theory and Applications*, Vol. 42, No. 11, pp. 920–932, Nov. 1995.
- [25] Silva-Martinez, J., Sorge-Suner, J., "A CMOS Preamplifier for Electret Microphones," *Proceedings of the 38th Midwest Symposium on Circuits and Systems*, Vol. 2, pp. 1018–21, 1996.

- [26] Pluygers, A. C., "A Novel Microphone Preamplifier for Use in Hearing Aids," *Analog Integrated Circuits and Signal Processing*, Vol. 3, pp. 113–8, 1993.
- [27] Nicollini, G., Guardiani, C., "A 3.3-V 800-nVrms Noise, Gain-Programmable CMOS Microphone Preamplifier Using Yield Modeling Technique," *IEEE Journal of Solid-State Circuits*, Vol. 28, pp. 915–21, Aug. 1993.
- [28] Awipi, M., Al-Smadi, A., "Effect of Analog and Digital Signal Conditioning Filters on Signal to Noise Ratio," *Proceedings of the IEEE Southeastcon '91*, Vol. 1, pp. 65–9, 1991.
- [29] O'Halloran, M. G., Sarpeshkar, R., "A Low Open-Loop Gain High-PSRR Micropower CMOS Amplifier for Mixed-Signal Applications," *Proceedings of the IEEE International Symposium on Circuits and Systems*, Vol. 2, pp. 424–7, 2002.
- [30] G. Franklin, J. D. Powell, A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 5th Edition, Prentice Hall, 2005.
- [31] Baker, M. W., Sarpeshkar, R., "A low-power high-PSRR current-mode microphone preamplifier," *IEEE Journal of Solid State Circuits*, Vol. 38, No. 10, pp. 1671–8, Oct. 2003.
- [32] Stone, M. A., Moore, B. C. J., "Side effects of fast-acting dynamic range compression that affect intelligibility in a competing speech task," *Journal of the Acoustical Society of America*, Vol. 114, No. 2311, 2004.
- [33] Stone, M. A., Moore, B. C. J., Alcantara, J. I., Glasberg, B. R., "Comparison of different forms of compression on using wearable digital hearing aids," *Journal of the Acoustical Society of America*, Vol. 106, No. 6, Dec. 1999.
- [34] Zhak, S. M., Baker, M. W., Sarpeshkar, R., "A low-power wide dynamic range envelope detector," *IEEE Journal of Solid State Circuits*, Vol. 38, no. 10, pp. 1750–3, Oct. 2003.

- [35] Baker, M. W., Lu, T. K.-T., Sarpeshkar, R., "A low-power AGC with level-independent phase margin," *Proceedings of the 2004 American Control Conference*, Vol. 1, pp. 386-9, July. 2004.
- [36] Sarpeshkar, R., Baker, M. W., Salthouse, C., Sit, J.-J., Turicchia, L., Zhak, S., "An analog bionic ear processor with zero-crossing detection," *Proceedings of the International Solid-State Circuits Conference*, San Francisco, CA, No. 4.2, pp. 78-9, Feb. 2005.
- [37] Wee, K.-H., Sit, J.-J., Sarpeshkar, R., "Biasing techniques for subthreshold MOS resistive grids," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2164-7, May. 2005.
- [38] Sarpeshkar, R., Lyon, R. F., Mead, C. A., "A low-power wide-linear-range transconductance amplifier," *Analog Integrated Circuits and Signal Processing*, Vol. 13, No. 1/2, pp. 123-151, May/Jun. 1997.
- [39] de Lange, E. K., DeFeo, O., van Staveren, A., "Modelling differential pairs for low-distortion amplifier design," *Proceedings of the IEEE International Symposium on Circuits and Systems*, Vol. 1, pp. 261-4, May. 2003.
- [40] Sarpeshkar, R., Delbruck, T., Mead, C., "White noise in MOS transistors and resistors," *IEEE Circuits and Devices Magazine*, Vol. 9, No. 6, pp. 23-9, Nov. 1993.
- [41] Sarpeshkar, R., Salthouse, C., Sit, J.-J., Baker, M. W., Zhak, S., Lu, T. K.-T., Turicchia, L., Balster, S., "An ultra-low-power programmable analog bionic ear processor," *IEEE Transactions on Biomedical Engineering*, Vol. 52, No. 4, pp. 711-727, Apr. 2005.
- [42] Pickles, J. O., "An Introduction to the Physiology of Hearing," Academic Press, 2nd Ed., 1988.
- [43] Hotvet, D. A., "Automatic gain control for hearing aid," *US Patent*, USPTN 4,718,099, Jan. 5, 1988.

- [44] Sarpeshkar, R., O'Halloran, M., "Scalable hybrid computation with spikes," *Neural Computation*, Vol. 14, No. 9, pp. 2003–38, Sept. 2002.
- [45] Moore, B. C. J., Glasberg, B. R., "Growth of forward masking for sinusoidal and noise maskers as a function of signal delay; implications for suppression of noise," *Journal of the Acoustical Society of America*, Vol. 73, pp. 1249–59, April 1983.
- [46] Stone, M. A., Moore, B. C. J., Alcantara, J. I., Glasberg, B. R., "Comparison of different forms of compression using wearable digital hearing aids," *Journal of the Acoustical Society of America*, Vol. 106, pp. 3603–19, 1999.
- [47] Cowan, G. E. R., Melville, R. C., Tsvividis, Y. P., "A VLSI analog computer/math co-processor for a digital computer," *IEEE International Solid-State Circuits Conference 2005*, pp. 82–3, Feb. 2005.
- [48] Nabelek, I. V., "Performance of hearing-impaired listeners under various types of amplitude compression," *Journal of the Acoustical Society of America*, Vol. 74, no. 3, Sept. 1983.
- [49] Baker, M. W., Sarpeshkar, R., "Low-Power Single-Loop and Dual-Loop AGCs for Bionic Ears," *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 9, pp. 1983–96, Sept. 2006.
- [50] Ricker, D. W., "Nonlinear feedback system for the normalization of active sonar returns," *Journal of the Acoustical Society of America*, Vol. 59, no. 2, 1977.
- [51] Arden, W., Fukushima, T., Kang, H.-K., Hu, C., Apte, P., "Overall roadmap technology characteristics," *International Technology Roadmap for Semiconductors*, 2004.
- [52] Rabii, S., Wooley, B., "A 1.8V digital-audio sigma-delta modulator in 0.8 –  $\mu\text{m}$  CMOS," *IEEE Journal of Solid State Circuits*, Vol. 32, no. 6, pp. 783–96, Jun. 1997.

- [53] Scott, M. D., Boser, B. E., Pister, K. S. J., "An ultralow-energy ADC for smart dust," *IEEE Journal of Solid State Circuits*, Vol. 38, no. 7, pp. 1123-29, Jul. 2003.
- [54] Russell, I. J., E. Murugasu, E., "Medial efferent inhibition suppresses basilar membrane responses to near characteristic frequency tones of moderate to high intensities," *Journal of the Acoustical Society of America*, Vol. 102, no. 3, Sept. 1997.
- [55] Dallos, P. J., "Dynamics of the acoustic reflex: Phenomenological aspects," *Journal of the Acoustical Society of America*, Vol. 36, no. 11, Sept. 1964.
- [56] Hamacher, Y., "Comparison of advanced monaural and binaural noise reduction algorithms for hearing aids," *IEEE Conference on Acoustics, Speech and Signal Processing.*, Vol. 4, pp.4008-11, May. 2002.
- [57] Deiss, A., Huang, Q., "A low-power 200-MHz receiver for wireless hearing aid devices," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 5, May. 2003.
- [58] Buchegger, T., Ossberger, G., Hochmair, E., Folger, U., Resenzahn, A., Springer, A., "An ultra-low power transcutaneous impluse radio link for cochlear implants," *International Workshop on Ultra Wideband Systems and Ultrawideband Systems and Technologies*, pp.356-60, May. 2004.
- [59] Baker, M. W., Sarpeshkar, R., "Feedback Analysis and Design of RF Power Links for Low-Power Bionic Systems," *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 1, No. 1, pp. 28-38, Mar. 2007.
- [60] J.-J. Sit, A. M. Simonson, A. J. Oxenham, M. A. Faltys, R. Sarpeshkar, "A low-power asynchronous interleaved sampling algorithm for cochlear implants that encodes envelope and phase information," *IEEE Transactions on Biomedical Engineering*, in press, expected publication January 2007.

- [61] P. R. Troyk, M. A. K. Schwan, "Closed-loop class-E transcutaneous power and data link for microimplants," *IEEE Transactions on Biomedical Engineering*, Vol. 39, No. 6, pp. 589-599, June 1992.
- [62] N. de N. Donaldson, T. A. Perkins, "Analysis of resonant coupled coils in the design of radio frequency transcutaneous links," *Medical and Biological Engineering and Computing*, Vol. 21, No. 5, Sept. 1983. pp. 612-627.
- [63] C. M. Zierhofer, E. S. Hochmair, "High-efficiency coupling-insensitive transcutaneous power and data transmission via an inductive link," *IEEE Transactions on Biomedical Engineering*, Vol. 37, No. 7, July 1990. pp 716-722.
- [64] G. Wang, W. Liu, M. Sivaprakasam, G. A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *IEEE Transactions on Circuits and Systems*, Vol. 52, No. 10, Oct. 2005, pp. 2109-2117.
- [65] F. E. Terman, *Radio Engineers Handbook*, New York: McGraw-Hill, 1943.
- [66] C. M. Zierhofer, E. S. Hochmair, "Coil design for improved power transfer efficiency in inductive links," *IEEE Engineering Medicine and Biology Society, 18th Annual International Conference*, 1996. pp 1538-9.
- [67] N. O. Sokal, A. D. Sokal, "Class-E - A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 10, Issue 3, June 1975, Pp. 168-176.
- [68] C. Fernandez, O. Garcia, J. A. Cobos, J. Uceda, "A simple dc-dc converter for the power supply of a cochlear implant," *IEEE 34th Annual Power Electronics Specialist Conference*, Vol. 4, June 2003. pp 1965-1970.
- [69] Morris, L. R., Barszczewski, P., "Design and evolution of a powerful pocket-sized DSP speech processing system for cochlear implant and other hearing prosthesis applications," *International Conference on Acoustics, Speech and Signal Processing*, pp. 2516 - 9, Apr. 1988.

- [70] McDermott, H. J., Vandali, A. E., van Hoesel, R. J. M., McKay, C. M., Harrison, J. M., Cohen, L. T., "A portable programmable digital sound processor for cochlear implant research," *IEEE Transactions on Rehabilitation Engineering*, Vol. 1, No. 2, pp. 94 - 100, Jun. 1993.
- [71] Bates, J. B., Gruzalski, G. R., Luck, C. F., "Rechargeable solid state lithium microbatteries," *Micro Electro Mechanical Systems 1993, Proceedings*, pp. 82-6, Feb. 1993.
- [72] Salthouse, C. D., Sarpeshkar, R., "A practical micropower programmable band-pass filter for use in bionic ears," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 1, Nov. 2003.
- [73] Sit, J.-J., Sarpeshkar, R., "A micropower logarithmic A/D with offset and temperature compensation," *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 2, Feb. 2004.
- [74] LTC3405A - Synchronous Step-Down Regulator *Linear Technology Corporation*, 2006.
- [75] El-Hamamsy, S.-A., "Design of High-Efficiency RF Class-D Power Amplifier," *IEEE Transactions on Power Electronics*, Vol. 9, No. 3, May. 1994.
- [76] Ramadass, Y. K., Chandrakasan, A. P., "Minimum Energy Tracking Loop with Embedded DC-DC Converter Delivering Voltages down to 250mV in 65nm CMOS," *Proceedings of the International Solid-State Circuits Conference*, San Francisco, CA, No. 3.2, pp. 64-5, Feb. 2007.